AIR FORCE T.O. 31M1-2FMQ13-1
ARMY TM 11-6660-282-10

TECHNICAL MANUAL

OPERATION INSTRUCTION MANUAL

WIND MEASURING SET
AN/FMQ-13(V)

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1 SEPTEMBER 1993
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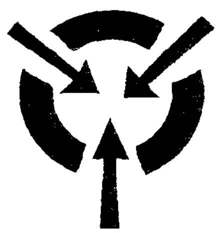
This manual provides operation instructions for the AN/FMQ-13(V) Digital Wind Measuring Set. This information is presented in three chapters. Chapter 1 starts with an introduction followed by a description of the equipment and a description of its application. The chapter ends with the leading particulars for the set. Chapter 2 has three sections. Section I describes the controls and displays. Section II contains the operating instructions. Section III covers emergency operation. Chapter 3 provides theory of operation in three sections. Section I provides an overview of the set and the components of the set. Section II covers the functional operation of the electronic circuits.

SAFETY SUMMARY

The following are general safety precautions that are not related to any specific procedures and therefore do not appear elsewhere in this publication. These are recommended precautions that personnel must understand and apply during many phases of operation and maintenance.

ELECTROSTATIC DISCHARGE SENSITIVE DEVICES. This equipment may contain electro-static discharge sensitive (ESDS) devices. Equipment handling methods and materials must be used to prevent equipment damage. Refer to Air Force Technical Order OO-25-234, Section VII, before disassembly, repair and assembly is performed for safety precautions. The requirements for marking assemblies, sub-assemblies and parts are governed by MIL STD 1686A, DOD HDBK 263, MIL STD 1285A and MIL STD 129.



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CAUTION - When installing the paper access cover onto the printer chassis assembly the grommets of the latches must be completely inserted into the latch holes of the printer chassis assembly. Be certain that the back of the access cover butts up against the flange of the printer chassis assembly before pushing the plunger in to expand the grommet. Failure to do so can cause the latch grommet to be damaged creating an ineffective latch.

CHAPTER 1

GENERAL INFORMATION

1-1 INTRODUCTION.

1-1.1 **Purpose and Scope of Technical Order**. This technical order contains instructions for operating Wind Measuring Set AN/FMQ-13(V) (hereinafter referred to as wind measuring set), manufactured by The Sutron Corporation, Herndon, Virginia. The technical order is arranged as follows:

Chapter 1 - General Information. This chapter provides general information for the wind measuring set including system application, equipment description, leading particulars, equipment supplied, and related technical manuals.

Chapter 2 - Operation. This chapter provides complete operating instructions for the wind measuring set.

Chapter 3 - Theory of Operation. This chapter discusses the theory of operation for the wind measuring set.

1-1.2 **Purpose of System**. The wind measuring set is intended for use in military base weather stations and on flight lines worldwide to continuously measure, display, and record horizontal wind speed, wind direction, and wind gust information.

1-1.3 **System Configuration**. The wind measuring set (FIGURE 1-1) consists of the following major assemblies:

Common Name	Official Nomenclature
Wind Measuring Set	Wind Measuring Set AN/FMQ-13(V)
Sensor	Sensor, Standard, Wind Measuring ML-660/FMQ-13(V).
Sensor	Sensor, Ruggedized, Wind Measuring ML-660A/FMQ-13(V).
Indicator	Digital Display Indicator ID-2408/FMQ-13(V)
Recorder	Wind Direction and Speed Recorder RO-588/ FMQ-13(V)

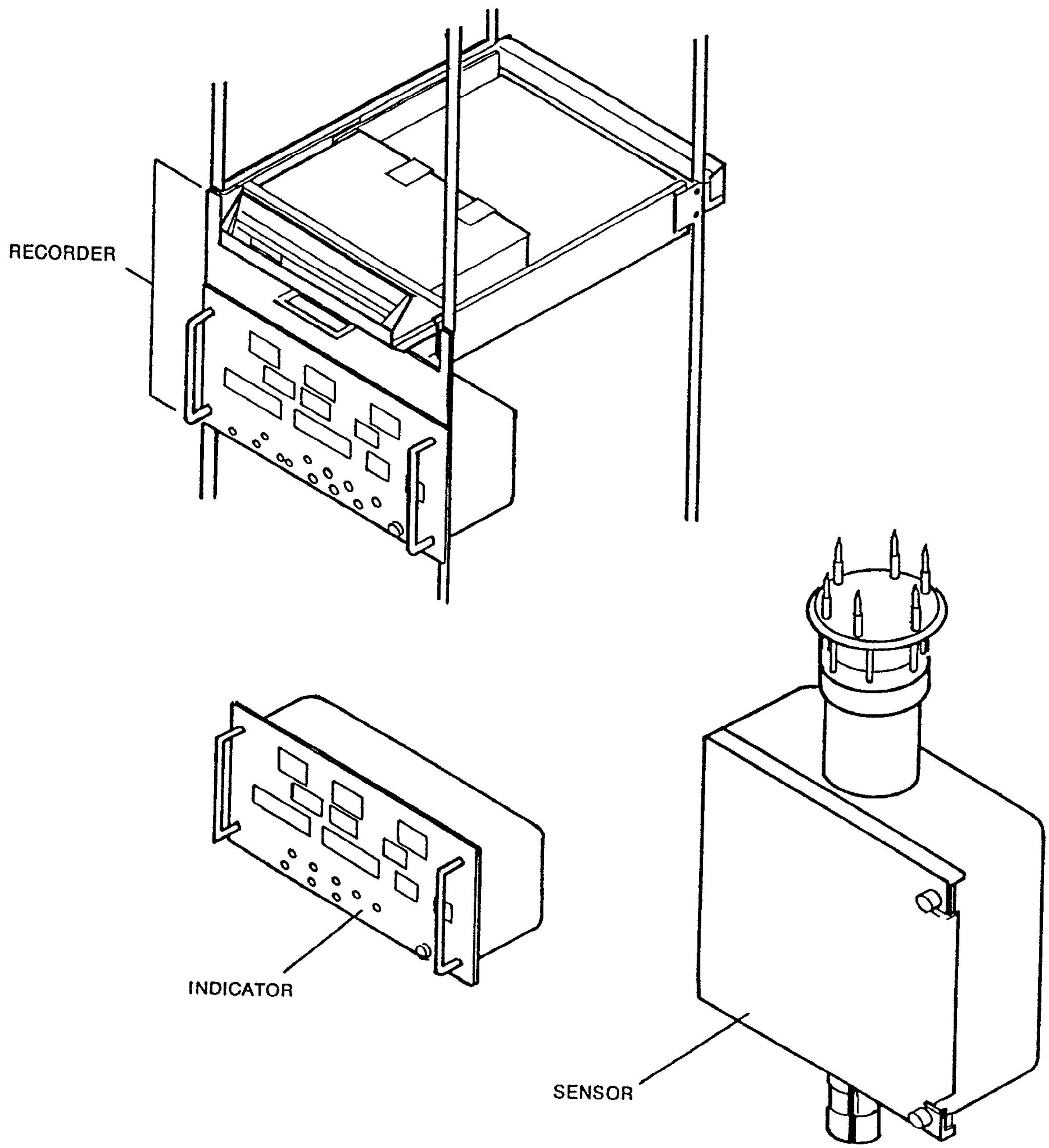


FIGURE 1-1. Wind Measuring Set AN/FMQ-13(V)

1-2 EQUIPMENT DESCRIPTION.

Refer to paragraphs 1-2.1 through 1-2.3 for a description of the equipment comprising the wind measuring set. A system can be comprised of these assemblies in various combinations as described in paragraph 1-3. A brief description of these assemblies is given in the following paragraphs.

1-2.1 **Sensor**. (See FIGURES 1-2, 1-3 and 1-4.) ~~The wind measuring set can be configured with either a standard sensor or ruggedized sensor.~~ ~~Both~~ The sensor~~s~~ provide the capability of measuring wind direction from 0 to 360 degrees~~. In addition, the ruggedized sensor provides the capability of measuring wind speed from 0 to 150 knots, while the standard sensor~~ and provides the capability of measuring wind speed from 0 to 99 knots. ~~Both~~ The sensor~~s~~ ~~are identical except for the~~ Erasable Programmable Read Only Memory (EPROM), which contains the temperature vs resistance data of the elements, temperature vs voltage data of the temperature circuit, voltage vs barometric pressure relationship of the barometric pressure circuit, gains and offsets for the digital-to-analog (D/A) and analog-to-digital (A/D) converters, and the calibration data for the sensor. ~~The EPROM in the ruggedized sensor is characterized over a wider range~~ of performance characteristics ~~allowed by~~ the ~~ability of the sensing elements to accurately measure winds above 99 knots.~~

~~Each~~ The sensor (FIGURE 1-2) consists of a control assembly and a power assembly. The control assembly (FIGURE 1-3) includes two microprocessor printed circuit board assemblies (PCBAs) and a heated protective cage, which protects two orthogonal thick-film platinum element pairs (X and Y). The X pair of elements is the East-West pair. The Y pair of elements is the North-South pair. By using two pairs of elements at right angles to each other, it is possible to calculate wind speed and direction.

A protective cage surrounds the sensing elements. The cage contains a heater which keeps ice from forming on the cage and obstructing the flow of air across the elements.

The elements are maintained at a temperature approximately 100 degrees C above ambient. As the wind blows across the elements, heat is removed and more power is required to maintain the elevated temperature. The power required to maintain a constant temperature is measured by the sensor electronics, and the wind velocity is calculated from these measurements.

When the control assembly is mounted to the power assembly, the two microprocessor PCBAs that form the control assembly will be fitted through the sensor support (FIGURE 1-4) into the power assembly watertight enclosure, where they are firmly seated to prevent shock and vibration.

The power assembly (FIGURE 1-4) includes a watertight enclosure which houses two PCBAs (power-front and power-back), both of which contain the sensor power supply and communications circuits, a circuit breaker assembly, a transformer assembly, and a terminal block with cover. The sensor is mounted onto a 1-inch pipe using a U-bolt for compression. Electrical connections to the sensor are made to the terminal block in the power assembly watertight enclosure.

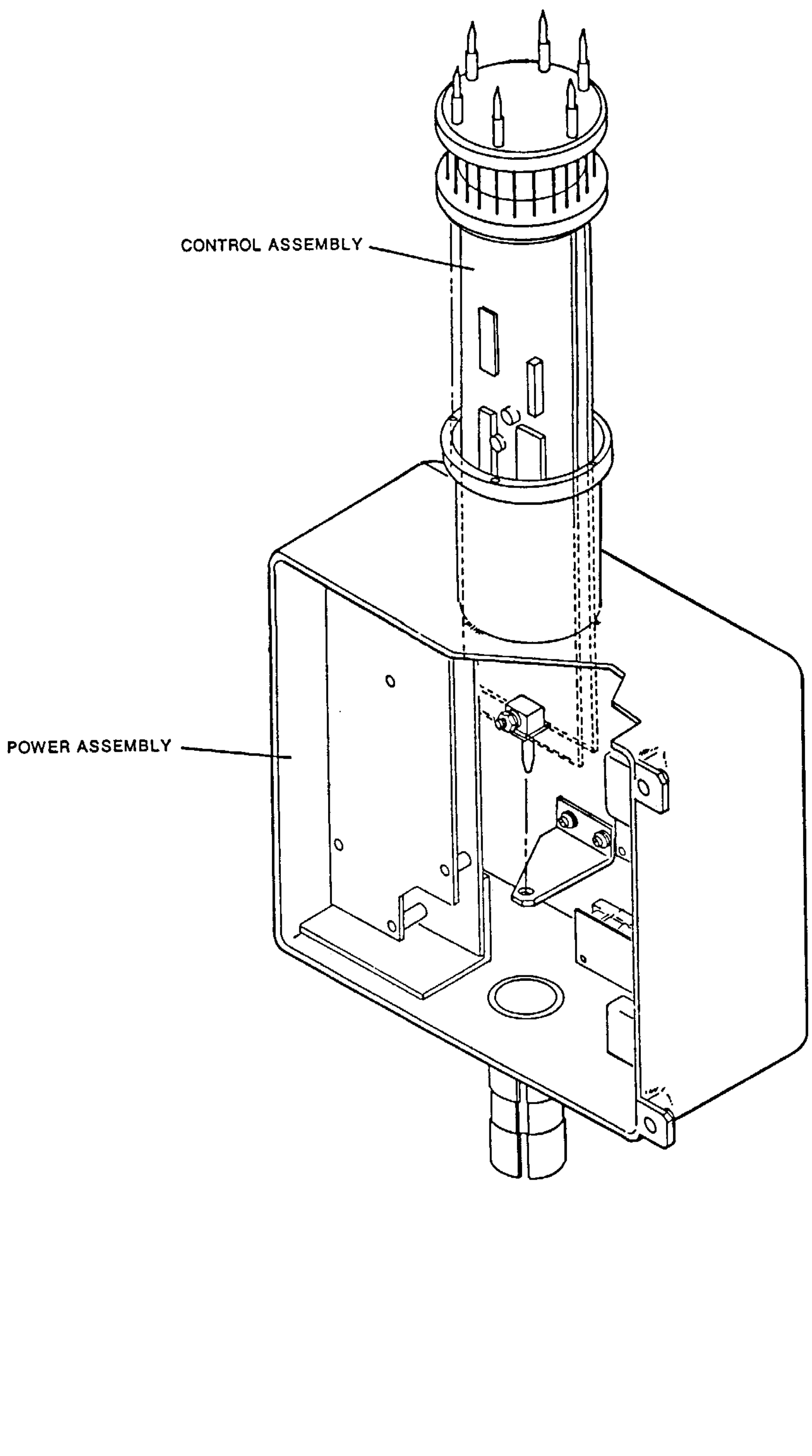


FIGURE 1-2. Wind Speed and Direction Sensor

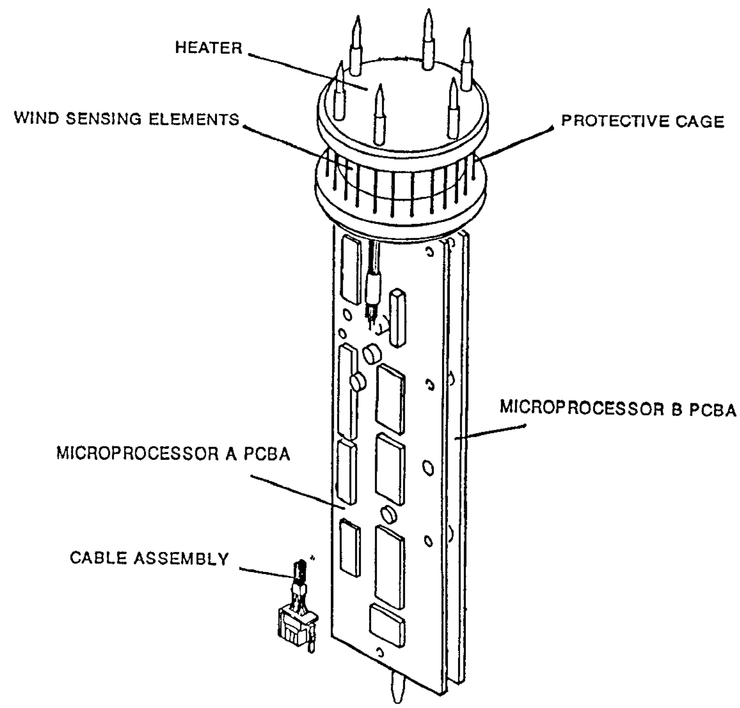


FIGURE 1-3. Wind Speed and Direction Sensor, Control Assembly

1-2.2 **Indicator**. (See FIGURES 1-5 and 1-6.) The wind measuring set uses two versions of the indicator (dash 1 and dash 2). The dash 1 version is a stand-alone indicator. The dash 2 version forms part of the recorder and is identical to the dash 1 indicator except for the addition of two connectors (AC POWER OUT and PRINTER) on the rear panel and minor changes to the display PCBA, interconnection PCBA, and front panel designations.

Each indicator is comprised of a top cover assembly (with EMI gasket), display panel, two handles, circuit breaker assembly, display intensity adjust potentiometer, pushbuttons/lamps, 7-segment displays, EMC window, communications cable assembly, configuration switch assembly, AC output cable assembly (dash 2 only), interconnection PCBA, microprocessor PCBA, display PCBA, and a display chassis which mounts a power transformer and two voltage regulators. The 7-segment displays, pushbuttons, and lamps visible through the panel are part of the display PCBA. Their function, as well as the function of all operator controls, visual displays/lamps, and connectors, is described in Chapter 2. All switches, displays/lamps, voltage regulators, power transformer, and other components mounted on the front and rear panels and display chassis are interfaced to the indicator electronics and power supply circuits via the interconnection PCBA.

The indicator (both dash 1 and dash 2 versions) provides readouts of wind information (wind direction, wind speed, gusts, direction variability, gust spread) processed from 5-second averages received from all sensors. The processed information is displayed on 7-segment displays on the indicator front panel along with the time and date, active sensor identification, and fault status. The indicator is designed for mounting either in a standard 19-inch rack or into a CY-2732/GMQ-20 Indicator Case.

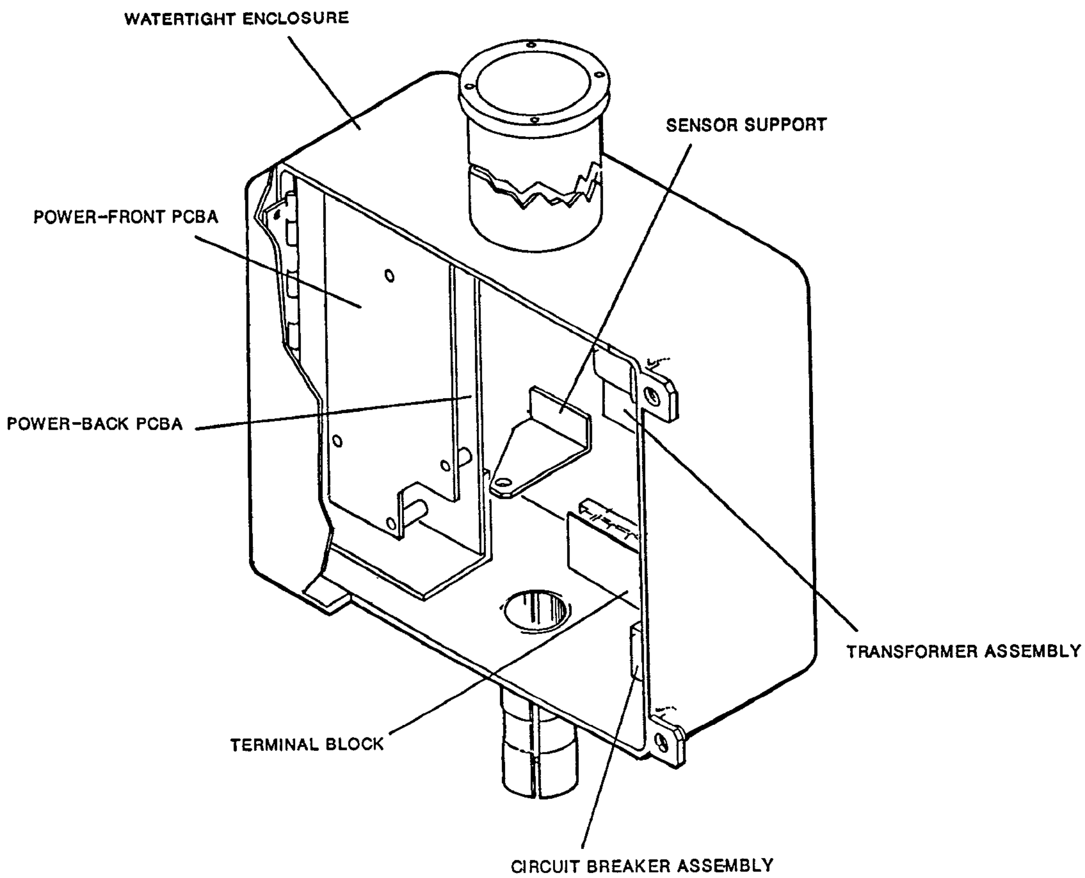


FIGURE 1-4. Wind Speed and Direction Sensor, Power Assembly

1-2.3 **Recorder**. (See FIGURES 1-7 and 1-8.) The recorder (FIGURE 1-7) is comprised of an indicator (dash 2 version), printer with slide mounting shelf, paper tray, paper access cover, AC power cable assembly, printer power cable assembly, and printer interface cable assembly. The printer shelf is equipped with captive hardware for slide mounting in a standard 19-inch equipment rack. Once each minute, the printer provides a hard-copy printout of all wind parameters displayed on the 7-segment displays plus time/date information, peak-wind values, standard deviation, status, and active sensor. All information for each minute's recording will be printed out on the same line. The order of presentation of the data will be as follows (see FIGURE 1-8): date; time; wind direction (DIR); wind speed (SPD), gusts (GST); direction variability (DIR-VAR); gust spread (GSP); 10-minute peak-wind direction, speed, and time of occurrence; latest hour peak-wind direction, speed, and time occurrence; latest 24-hour peak-wind direction, speed, and time of occurrence; standard deviation (SD); active-sensor identification (AS); and status (ST). Header information is provided on the printout to clearly identify all recorded information. All time is based on a 24-hour clock and is displayed to the latest minute. Wind data to be recorded will be from the sensor specified as the active sensor on the master indicator. FIGURE 1-8 is a typical printout of weather information.

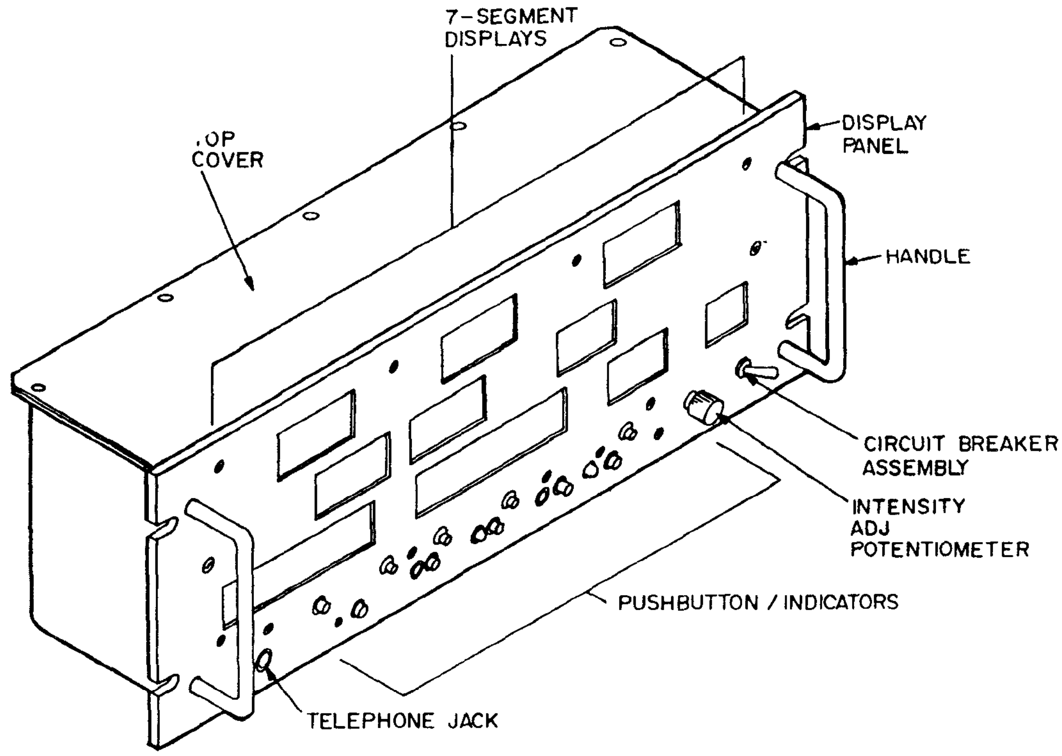


FIGURE 1-5. Digital Display Indicator ID-2408/FMQ-13(V), Front View

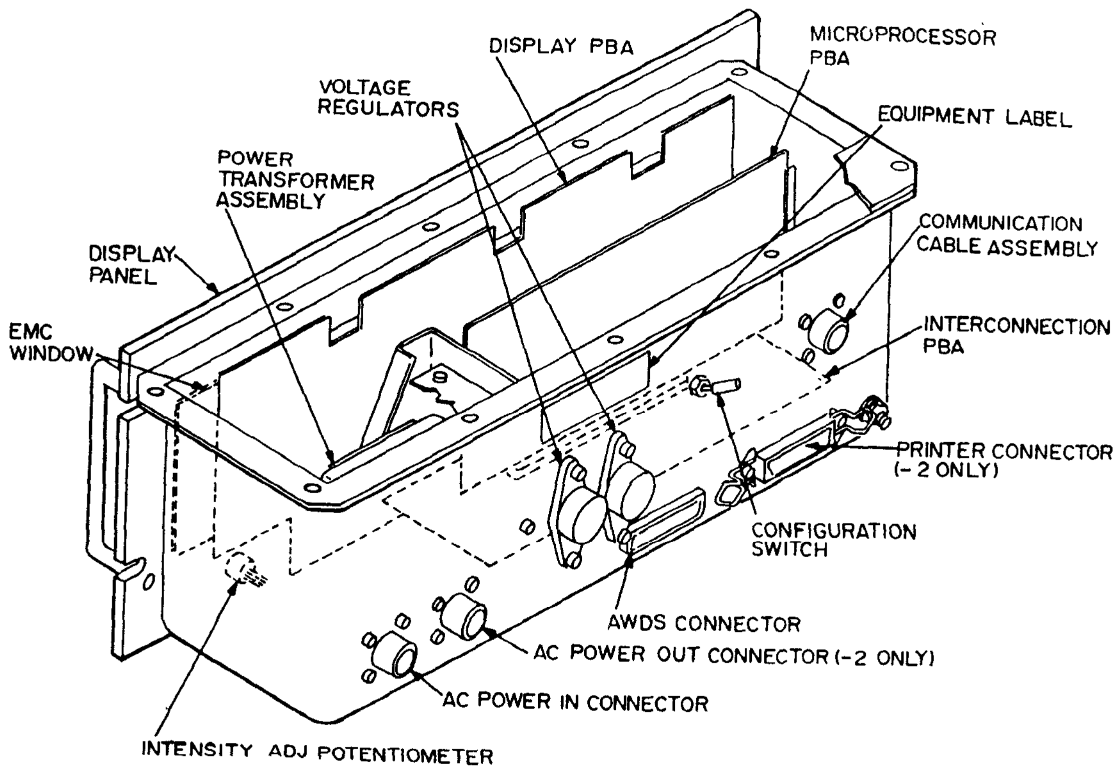


FIGURE 1-6. Digital Display Indicator ID-2408/FMQ-13(V), Rear View

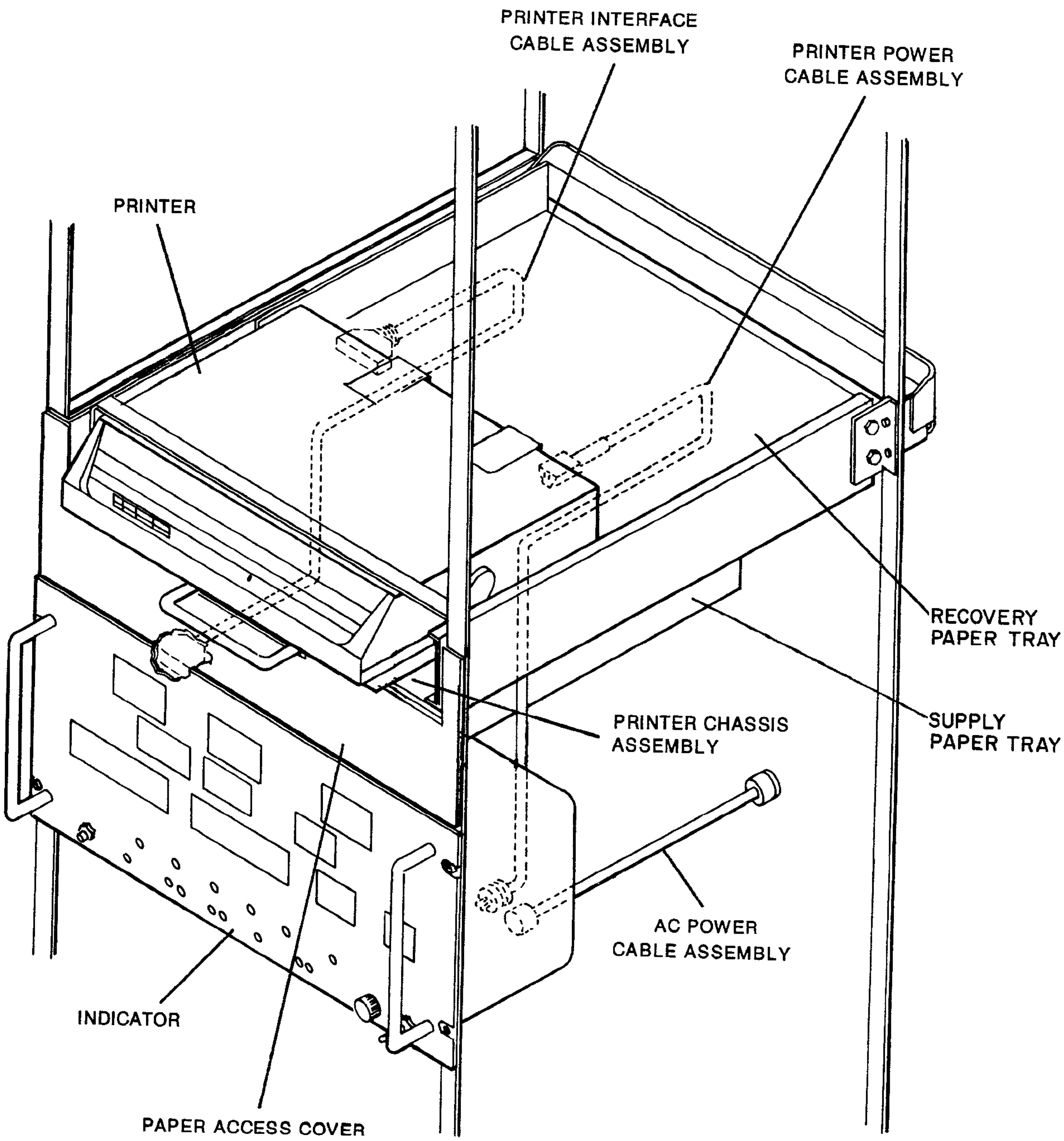


FIGURE 1-7. Wind Direction and Speed Recorder RO-588/FMQ-13(V)

								10 MIN. PEAK			60 MIN. PEAK			24 HOUR PEAK					
DATE	TIME	DIR	SPD	GST	DIR -	VAR	GSP	DIR	SPD	TIME	DIR	SPD	TIME	DIR	SPD	TIME	SD	AS	ST
01/07/89	15:44	344	001	000	084	359	001	112	003	15:34	136	005	14:09	343	011	03:08	060	01	00
01/07/89	15:45	306	002	000	084	359	002	280	005	15:44	136	005	14:09	343	011	03:08	060	01	00
01/07/89	15:46	290	004	000	084	359	001	282	005	15:45	136	005	14:09	343	011	03:08	055	01	00
01/07/89	15:47	291	005	000	091	359	001	291	005	15:46	136	005	14:09	343	011	03:08	050	01	00
01/07/89	15:48	295	005	000	179	359	001	291	005	15:46	136	005	14:09	343	011	03:08	044	01	00
01/07/89	15:49	296	005	000	184	359	001	296	005	15:48	136	005	14:09	343	011	03:08	032	01	00
01/07/89	15:50	290	005	000	259	359	001	296	005	15:48	136	005	14:09	343	011	03:08	024	01	00
01/07/89	15:51	283	005	000	259	359	001	286	006	15:50	136	005	14:09	343	011	03:08	018	01	00
01/07/89	15:52	275	005	000	256	359	001	279	006	15:51	136	005	14:09	343	011	03:08	018	01	00
01/07/89	15:53	274	004	000	256	355	001	279	006	15:51	136	005	14:09	343	011	03:08	018	01	00
01/07/89	15:54	274	003	000	256	305	002	279	006	15:51	136	005	14:09	343	011	03:08	014	01	00
01/07/89	15:55	276	004	000	256	304	001	279	006	15:51	279	006	15:51	343	011	03:08	010	01	00
01/07/89	15:56	275	004	000	254	304	002	279	006	15:51	279	006	15:51	343	011	03:08	010	01	00
01/07/89	15:57	268	003	000	251	304	002	279	006	15:51	279	006	15:51	343	011	03:08	011	01	00
01/07/89	15:58	267	003	000	251	302	002	279	006	15:51	279	006	15:51	343	011	03:08	012	01	00
01/07/89	15:59	267	003	000	251	302	002	279	006	15:51	279	006	15:51	343	011	03:08	011	01	00
01/07/89	16:00	263	003	000	242	291	002	279	006	15:51	279	006	15:51	343	011	03:08	010	01	00
01/07/89	16:01	266	003	000	242	289	001	279	006	15:51	279	006	15:51	343	011	03:08	010	01	00
01/07/89	16:02	276	003	000	242	297	001	282	005	15:54	279	006	15:51	343	011	03:08	009	01	00
01/07/89	16:03	281	003	000	242	297	001	282	005	15:54	279	006	15:51	343	011	03:08	010	01	00
01/07/89	16:04	289	003	000	242	303	001	282	005	15:54	279	006	15:51	343	011	03:08	010	01	00
01/07/89	16:05	288	003	000	242	303	001	271	004	15:55	279	006	15:51	343	011	03:08	012	01	00
01/07/89	16:06	285	003	000	242	303	000	264	004	15:56	279	006	15:51	343	011	03:08	012	01	00
01/07/89	16:07	287	003	000	242	305	001	262	004	15:57	279	006	15:51	343	011	03:08	012	01	00
01/07/89	16:08	297	003	000	242	318	001	287	004	16:04	279	006	15:51	343	011	03:08	012	01	00
01/07/89	16:09	314	003	000	242	341	001	287	004	16:04	279	006	15:51	343	011	03:08	011	01	00
01/07/89	16:10	318	003	000	265	341	002	287	004	16:04	279	006	15:51	343	011	03:08	011	01	00
01/07/89	16:11	304	003	000	265	341	001	287	004	16:04	279	006	15:51	343	011	03:08	009	01	00
01/07/89	16:12	306	003	000	273	341	002	316	004	16:11	279	006	15:51	343	011	03:08	009	01	00
01/07/89	16:13	305	003	000	273	341	001	316	004	16:11	279	006	15:51	343	011	03:08	009	01	00

FIGURE 1-8. Typical Printout of Weather Information

The printer provides the ASCII 96 character set with upper and lower case characters and true descenders, double width, and enhanced print characters. The printer is provided with a re-inking ribbon cartridge which delivers crisp quality up to 3 million characters.

A plate at the top rear of the printer provides access to DIP switches which allow selection of printer function. These switches control selection of language characters, the form length setting, line feed options, and must be set to match the protocol used by the microprocessor PCBA in the indicator which uses eight-bit character bytes.

The recorder is equipped with an audible alarm to alert base weather station personnel when the active sensor is changed. The alarm has a manual reset switch on the front panel of the recorder to allow the operator to reset the alarm.

1-3 **SYSTEM APPLICATION**. (See FIGURE 1-9.)

The wind measuring set is comprised of three basic major assemblies: sensor, indicator, and recorder. A minimum system consists of one sensor and one indicator or recorder. A maximum system consists of up to four sensors and a total of up to sixteen indicators and/or recorders. The sensors are mounted on masts at the end of up to four runways on the base. Typically, the indicators are located at air traffic control and weather facilities, and recorders are located with the base weather station observer.

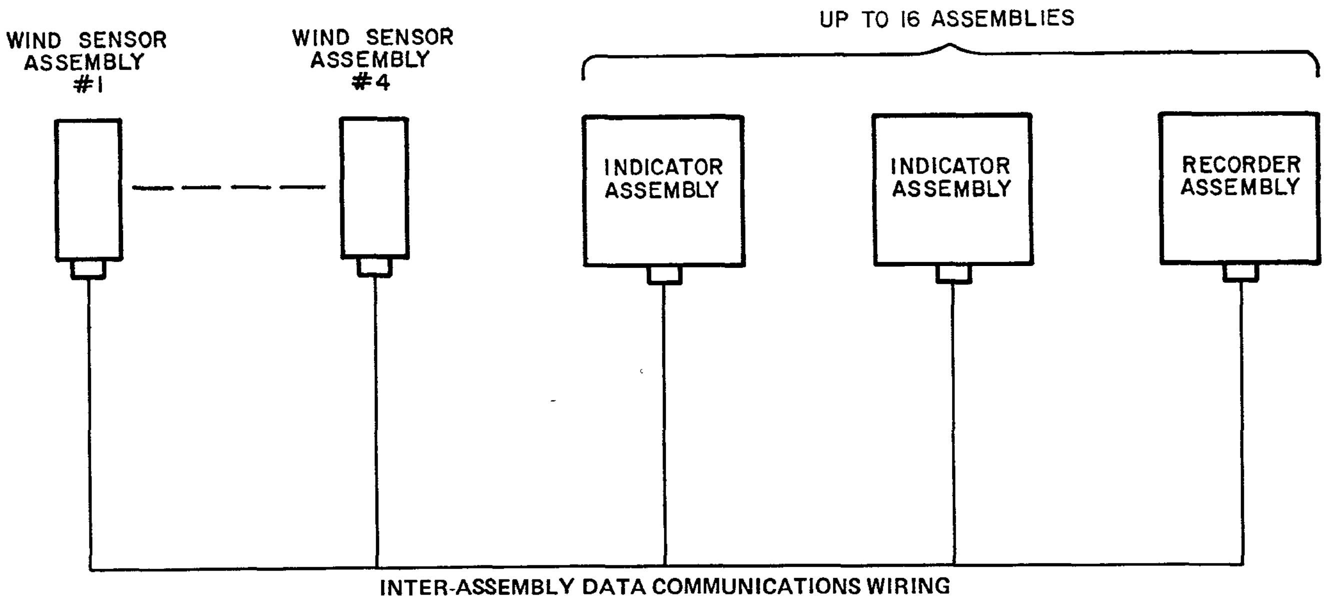


FIGURE 1-9. Wind Measuring Set, Overall Block Diagram

~~Both~~ The sensors ~~(standard and ruggedized)~~ provides the capability of measuring wind direction from 0 to 360 degrees. ~~In addition, the ruggedized sensor provides the capability of measuring wind speed from 0 to 150 knots; while~~ the standard sensor provides the capability of measuring wind speed from 0 to 99 knots. Wind samples taken over a 5-second period are grouped and vectorially averaged. These 5-second averaged values are used by the indicators and recorders to calculate and display/record further wind information.

One, and only one, of the possible sixteen indicators and/or recorders in the system is designated as the "master" by means of a switch on the rear panel of that unit.

The master indicator/recorder polls all sensors every 5 seconds. When polled, wind velocity information from all sensors is simultaneously transmitted to all indicators and recorders in the system over the inter-assembly data communications channel. Data from the active sensor is displayed on all indicators unless the operator momentarily selects display of wind information from another sensor. The inter-assembly data communications channel usually consists of a single dedicated pair of wires, up to 20,000 feet long, running between all assemblies on a single air base; however, a 3002-type two-wire private line data channel may be used in addition to, or in place of, the dedicated wires to accommodate much longer distances between assemblies.

The inter-assembly data communications channel allows the four sensors and up to sixteen indicators/recorders to be tapped into a single pair of wires. Thus, the wind speed and wind direction information from each addressed sensor is fed simultaneously to all indicators and recorders in the system.

Each indicator and recorder vectorially averages 5-second wind velocity information from up to four sensors to provide numerical readouts (degrees or knots) for wind direction and speed, direction variability, gusts, and gust spread. This information is displayed on the 7-segment LED displays of both the indicators and recorders. In addition, the recorder provides a hard-copy printout of all weather parameters, including all parameters displayed on the 7-segment displays plus time/date information and additional weather data (like peak wind data) for the active sensor only.

Prior to updating each numerical readout on the indicator and recorder, the system built-in test (BIT) determines if there are any faults that would affect display accuracy. When a fault is detected, the last correct readings will remain unchanged and the wind data and status displays on the indicator or recorder sensing the fault will flash at a rate of 1.0 +/- 0.25 Hz. The flashing STATUS display will display a general status code. Pressing the STATUS CLEAR pushbutton will cause the STATUS display to stop flashing. However, the general error code will still be displayed if the fault remains. The operator can then select the STATUS DISPLAY mode by depressing the STATUS CLEAR pushbutton while holding the LAMP TEST pushbutton depressed. This causes all displays to be blanked except the four that display a specific error code. With the status mode selected, the TIME display flashes all zeros to alert the operator that the indicator/recorder is not in its normal operating mode.

Each indicator and recorder provides the capability of communicating with an automated system via the Automated Weather Distribution System (AWDS) interface. At the end of each 5-second update of the active sensor, the following data for each sensor is available for transmission from each indicator and recorder: system nomenclature header; date-time group; wind direction; wind speed; gusts; direction variability; gust spread; 10-minute peak-wind direction, speed, and time of occurrence; 60-minute peak-wind direction, speed, and time of occurrence; latest 24-hour peak-wind direction, speed, and time of occurrence; standard deviation; active sensor identification; and status code.

FIGURE 1-10 provides an example of the AWDS message and shows the location of each data field. Table 1-1 provides a description of each field, the range of values that the field can contain, the length of each field, and the field start position for each field.

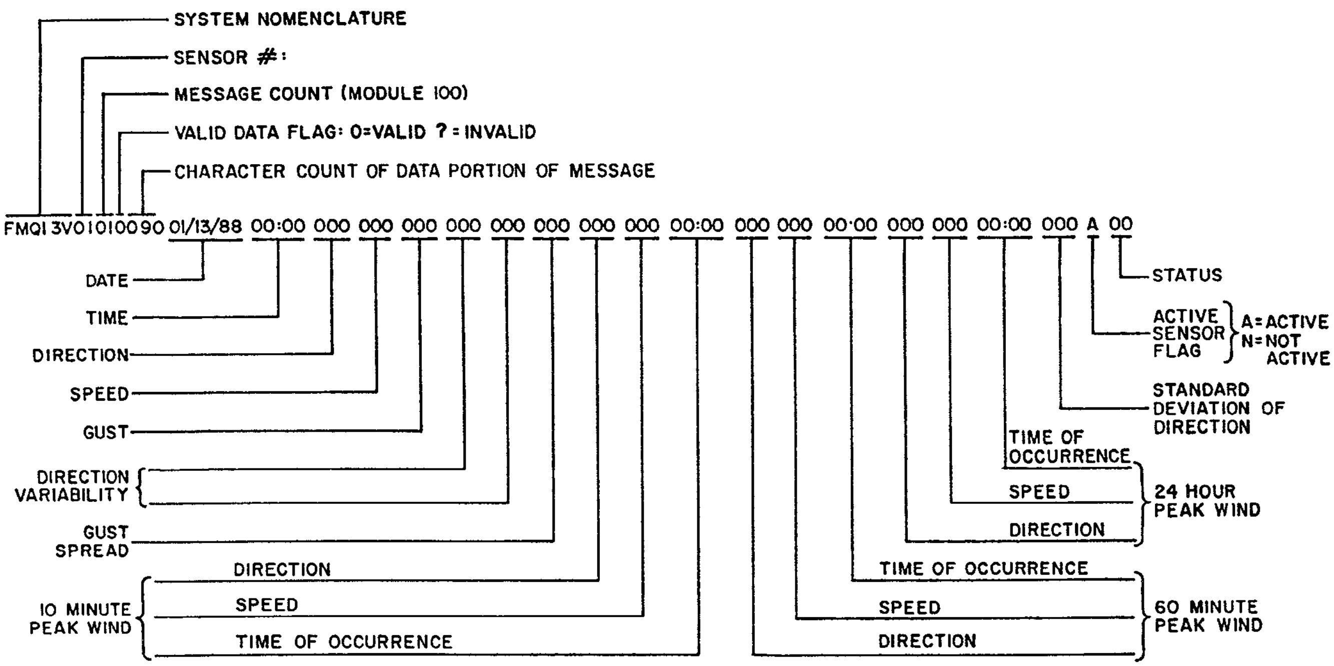


FIGURE 1-10. AWDS Message

Table 1-1. AWDS Output Format

Field Name	Content	Field Length	Field Position
System Nomenclature	FMQ13(V)	6	1
Sensor #	01-04	2	7
Message Count (Modulo 100)	00-99	2	9
Valid Data Flag	? or 0	1	11
Character Count	090	3*	12
Meteorological Data:			
Date	MM/DD/YY	8*	16
Time	HH:MM	5*	25
Wind Direction	000-360	3*	31

Table 1-1. AWDS Output Format - CONT

Field Name	Content	Field Length	Field Position
Meteorological Data:			
Wind Speed	000-250	3*	35
Gust	000-250	3*	39
Direction Variability 1	000-360	3*	43
Direction Variability 2	000-360	3*	47
Gust Spread	00-99	3*	51
10-Minute Peak Wind Direction	000-360	3*	55
10-Minute Peak Wind Speed	000-250	3*	59
10-Minute Peak Time	HH:MM	5*	63
60-Minute Peak Wind Direction	000-360	3*	69
60-Minute Peak Wind Speed	000-250	3*	73
60-Minute Peak Time	HH:MM	5*	77
24-Hour Peak Wind Direction	000-360	3*	83
24-Hour Peak Wind Speed	000-250	3*	87
24-Hour Peak Time	HH:MM	5*	91
Standard Deviation Direction	000-180	3*	97
Active Flag	N or A	1*	101
Status	00-77	2	103
Message Termination	CR-LF	2	105

* one space character follows these fields

1-4 LEADING PARTICULARS.

The exterior paint on the sensor is gloss medium gray and the paint on the mast is airfield orange, MIL-C-85285. The performance characteristics of the sensor can be degraded by improper paint application. The leading particulars of the wind measuring set are given in the following paragraphs:

1-4.1 Performance Characteristics.

1-4.1.1 System.

1-4.1.1.1 Operating Range.

Wind Speed.......	Calibrated measurement range. 0-99 knots ~~(standard sensor), 0-150 knots (ruggedized sensor)~~. ~~Both types of~~ sensors can withstand wind speed in excess of 150 knots
Wind Direction.......	0-360 degrees

1-4 1.1 2 Accuracy.

Speed.................	0-50 knots +/- 1 knot 50-75 knots +/- 5% 75-99 knots +/- 10% ~~99-150 knots +/- 15% (ruggedized only)~~
Direction..............	+/- 3 degrees

1-4 1.1.3 Sensitivity.

Constant Wind Speed .	As little as 1 knot
Shift in Wind Direction .	As little as 3 degrees shift in wind direction at a wind speed of 1 knot.
Primary Power......... Requirement	115/230 VAC +/- 10%, 47-63 Hz, single phase (all assemblies). 115/230 VAC is selectable by internal strapping.

1-4.1.2 Sensor Assembly.

1-4 1.2.1 Sensor Response Time.

Wind Speed............	Time required for sensors to respond to 63 percent of a 25 knot step change in wind speed in no less than 1 second and no more than 5 seconds
Wind Direction.........	Time required for sensors to respond to 63 percent of a 90 degree instantaneous shift in wind direction at a constant speed of 25 knots in no less than 1 second and no more than 5 seconds

Sensor Processing . . . The wind velocity is sampled at least once per second; these samples are grouped and vectorially averaged to create 5-second averaged values. The 5-second averaged values are then used by the indicator and recorder to calculate further wind information.

Built-in Self-Test (BIT) . Ensures that the sensor assemblies are performing as required. Fault indications are displayed on front panel of both indicator and recorder assemblies.

1-4.1.3 **Indicator Assembly**.

1-4.1.3.1 **Visual Display**.

Readability . . . . All visual displays have a viewing angle of +/- 60 degrees from the perpendicular in both horizontal and vertical axis.

Wind Direction . . . . . . Wind direction is displayed to the nearest degree. Display updated every 5 seconds.

Wind Speed . . . . Wind speed displayed to the nearest knot. Display updated every 5 seconds.

Gusts . . . . Maximum wind gusts within the past 10 minutes displayed to the nearest knot. Display updated every 5 seconds.

Direction Variability . . . Displayed by presenting two values ("XXX" to "YYY") which bracket in a direction the 5-second wind directions observed within the past 10 minutes. Display updated every 5 seconds. When direction variability exceeds 359 degrees the current wind direction value is displayed in both Direction Variability displays as well as the Wind Direction display.

Gust Spread . . . . Maximum wind gust within the past 1 minute displayed to the nearest knot. Display is updated every 5 seconds.

Time . . . . Displays real time in hours, minutes, and seconds.

Date . . . . Displays date in day, month, and year.

Status . . . . Flashes and displays an error code if the built-in-test has detected a failure. Indicates a malfunction in the sensor, indicator, or a communications failure.

Active Sensor Identification . . . . Active wind sensor display is changed on individual indicators when a different sensor is selected via the sensor selector switch on the master assembly.

Inter-Assembly Communications . . . . . . Indicator is provided with a MIL-J-641, type JJ-134 telephone jack for communication by maintenance personnel among sensor, indicator and recorder locations.

Momentary Wind Sampling Capability .... Each indicator has the capability of overriding the active sensor selector switch and momentarily displaying data from any of the other installed sensors. This momentary override capability automatically expires after 1 minute if not disabled sooner by the operator, and processed data from the active sensor is again displayed.

1-4.1.3.2 **Processing**.

Wind Data Processing . The indicator processes the following information from the 5-second vectorially averaged wind speed and wind direction values calculated by each sensor.

Wind Speed and Direction ..... Wind speed and wind direction readings are vectorially averaged over the past 2-minute period. Computed directions of 0 and 360 degrees are displayed as 360 degrees. Calm winds are displayed as 000 direction and 000 speed. Update of these 2-minute average values is made every 5 seconds.

Gusts .... Values for maximum gusts (to the nearest knot) measured within the past 10 minutes are calculated. When a gust spread of at least 10 knots has occurred and the 10-minute peak wind exceeds the current 2-minute average by 5 knots or more, the 10-minute peak wind will be displayed as the gust. Gusts are updated every 5 seconds. When no gusts are present, or the 2-minute wind is calm, the indicator will display all zeros.

Direction Variability ... The two extreme values of wind direction which bracket all wind directions are identified during the most recent 10-minutes of system operation and identified in a clockwise direction. Direction variability is updated every 5 seconds. When direction variability exceeds 359 degrees the current wind direction value is displayed in both Direction Variability displays as well as the Wind Direction display.

Gust Spread .... Maximum gust spread over the past minute is calculated. Gust spread is defined as the maximum difference between a 5-second wind speed peak and a 5-second wind speed lull. Gust spread is updated every 5 seconds.

Peak Wind .... Peak-wind value (in knots) over the most recent 10-minute, 60-minute, and 24-hour periods are calculated. Peak wind is defined as the highest 5-second average wind speed measured by the sensor along with its associated direction and time of occurrence. The 10-minute peak-wind speed is updated every 5 seconds. The latest hourly peak-wind and 24-hour peak-wind speed are updated at 55 minutes after the hour.

Standard Deviation of Wind Direction . The standard deviation of wind direction (to the nearest degree) over the most recent 10-minute period is calculated. This value is updated once a minute.

Automated Weather Distribution System (AWDS) Interface . . Each indicator provides the capability of communicating with an automated observing system via the AWDS interface. At the end of each 5-second update for each sensor, the following data is available for transmission from each indicator: date-time group; wind direction; wind speed; gusts; direction variability; gust spread; 10-minute peak-wind direction, speed, and time of occurrence; latest hourly peak-wind direction, speed, and time of occurrence; latest 24-hour peak-wind direction, speed and time of occurrence; standard deviation; active sensor identification; and status code. The interface follows the unbalanced generator-receiver configuration of MIL-STD-188-114. However, the capability is provided for wiring the optional grounding and balancing arrangements in MIL-STD-188-114 and for installing the voltage protection.

1-4.1.3.3 **Testing**.

Built-In Self-Test (BIT) . Prior to updating each numerical readout, the indicator tests itself for faults. When a fault is detected, the last correct readings will remain unchanged and the wind data and status displays will flash at a 1.0 +/- 0.25 Hz rate and an error code will be displayed in the STATUS display.

1-4.1.4 **Recorder Assembly**.

1-4.1.4.1 **Visual Displays**.

NOTE

The recorder visual displays (LEDs and printout) are updated once each minute on the minute. Processing of the 5-second wind data continues in the intervening time to maintain the wind data base and to support the AWDS output that occurs every 5 seconds.

Readability . . . . All visual displays have a viewing angle of +/- 60 degrees from the perpendicular in both horizontal and vertical axes.

Data Displayed . . . . . . Wind direction, wind speed, direction variability, gusts, and gust spread is identical to the indicator displays. The date-time group and active sensor identification are also displayed. In addition, the 10-minute, 60-minute, 24-hour peak-wind values and the standard deviation of wind direction can be displayed by use of the DISPLAY SELECT switches.

Time . . . . Displays real time in hours, minutes, and seconds.

Date . . . . Displays date in days, month, and year.

Status . . . . Flashes and displays an error code if the built-in-test has detected a failure. Indicates a malfunction in the sensor, recorder, or a communications failure.

Printout....... ... ... Once each minute, the recorder will printout all parameters displayed visually on the recorder, calculated peak-wind values, standard deviation, active sensor identification, status and the date-time group of the recording. All time is based on a 24 hour clock. Wind data to be recorded is calculated from the 5-second averages from the sensor specified by the active sensor selector switch.

Audible Alarm.......... Alerts base weather station personnel when the active sensor is changed

Inter-Assembly......... Communications Recorder is provided with a MIL-J-641, type JJ-134 telephone jack for communications by maintenance personnel among sensor, indicator and recorder locations.

1-4.1 4.2 **Processing.**

NOTE

The update periods mentioned in this section on processing refers to the data processing interval. The display update interval is as described in paragraph 1-4.1.4.1 (one each minute on the minute.)

Wind Data Processing.... The recorder processes the following information from the 5-second vectorially averaged wind direction and wind speed calculated by each sensor.

Wind Speed and........... Direction Wind speed and wind direction readings vectorially averaged over a 2-minute period (optional 10-minute period that is internally switchable by maintenance personnel)

Computed directions of 0 degrees and 360 degrees are displayed as 360 degrees. Calm winds are recorded as 000 direction and 000 speed. Update of these 2-minute average values made every 5 seconds. Displays are only updated once a minute even though the values are processed every 5 seconds.

Gusts....................... Values for maximum gusts (to the nearest knot) measured within the past 10 minutes are calculated. How gusts are calculated depends on whether the system is set up for 2- or 10- minute averaging. For systems set up for 2-minute averaging, the 10-minute peak wind will be displayed as the gust only when a gust spread of at least 10 knots has occurred and the 10-minute peak wind exceeds the current 2-minute average by 5 knots or more. For systems set up for 10-minute averaging, the gust is defined as the 10-minute peak wind only when the 10-minute peak wind exceeds the current 10-minute average by 5 knots or more. In each case, gusts are updated every 5 seconds. When no gusts are present, or the 2- (or 10-) minute wind is calm, the recorder will display and record all zeros.

Direction Variability...... Extreme values of wind direction which bracket all wind directions are identified during the most recent 10 minutes of system operation are identified in a clockwise direction. Updated every 5 seconds. When direction variability exceeds 359 degrees the current wind direction value is displayed in both Direction Variability displays as well as the Wind Direction display.

Gust Spread . . . . Maximum gust spread over the past minute is calculated. Gust spread is defined as the maximum difference between a 5-second wind speed peak and a 5-second wind speed lull. Gust spread is calculated every 5 seconds.

Peak Wind . . . . Peak-wind values (in knots) for the most recent 10-minute, 60-minute, and 24-hour periods are calculated. Peak wind is defined as the highest 5-second averaged wind speed measured by the sensor along with its associated direction and time of occurrence. The 10-minute peak-wind spread is updated every 5 seconds. The latest hourly and the latest 24-hour peak wind speed are updated at 55 minutes after the hour.

Standard Deviation of Wind Direction . The standard direction of wind direction (to the nearest degree) over the most recent 10-minute period is calculated. This value is updated once a minute.

Automated Weather Distribution System (AWDS Interface) . . Each recorder provides the capability of communicating with an automated observing system via the AWDS interface. At the end of each 5-second update for each sensor, the following data are available for transmission from each recorder: sensor number; date-time group; wind direction; wind speed; gusts; direction variability; gust spread; 10-minute peak-wind direction, speed, and time of occurrence; latest 60-minute peak-wind direction, speed, and time of occurrence; latest 24-hour peak-wind direction, speed, and time of occurrence; standard deviation; and active sensor identification; and status code. The interface follows the unbalanced generator-receiver configuration of MIL-STD-188-114. However, the capability is provided for wiring the optional grounding and balancing arrangements in MIL-STD-188-114 and for installing voltage protection.

1-4.1.4.3 **Testing**.

Built-In Self-Test (BIT) . Prior to updating each numerical readout, the recorder tests itself for faults. When a fault is detected, the last correct reading will remain unchanged and the fault display(s) will flash at a 1.0 +/- 0.25 Hz rate. An error code will be displayed in the STATUS display.

1-4.1.5 **Printer**.

Print Speed	
Utility Mode	120 cps
Print Technique	Bidirectional/short line seeking dot matrix impact
Interface	Parallel, Centronics compatible
Character Matrix (HxV)	9x9 inch Utility mode
Characters per line	137 characters @ 17.1 cpi

Media

Number of sheets	1 to 4 sheets
Maximum width of paper:	
Friction Feed	8.5"
Tractor feed	9.5"
Pin Feed	10"
Paper path	Rear/bottom
Ribbon	Okidata cartridge - re-inking

Power

Voltage	120, 220 or 240 VAC +/- 10%
Frequency	47 - 60 Hz
Power (operating)	35 watts

Format Controls

Vertical tabs

Top of Form Set

Horizontal Tabs

Skip Over Perforation

1-4.2 **Environmental Requirements**.

1-4.2.1 **Sensor Assemblies**.

Temperature:

Operating . . . . . . -51 to +68 degrees C

Non-operating . . -57 to +68 degrees C

Altitude:

Operating . . . . . . -100 to 15,000 feet

Non-operating . . -100 to 40,000 feet

Humidity	0 to 100% including condensation from -51 degrees C to 27 degrees C (81 degrees F). Above 27 degrees C, the relative humidity shall be based on a dew point of 27 degrees C.
Wind (Standard)	No deterioration of performance with peak winds of 99 knots or gusts of 90 knots with +/- 30 degree shift in wind direction within 10 seconds. The standard sensor will withstand the same peak winds as the ruggedized sensor (199 knots or gusts of 150 knots with +/- 60 degree shifts in wind direction within 10 seconds) without damage. Winds above 99 knots will cause an OUT OF RANGE status to be reported. No maintenance action is required for this condition.
Wind (Ruggedized) . . .	No damage when subjected to peak winds of 199 knots or gusts of 150 knots with +/- 60 degree shifts in wind direction within 10 seconds.
Ice, Sleet, and Snow . . (Standard)	No deterioration of performance with 90 knot wind with an inch of radial ice buildup on the mast.
Ice, Sleet, and Snow . . (Ruggedized)	No deterioration of performance with 150 knot wind with an inch of radial ice buildup on the mast.

1-4.2.2 **Indicator/Recorder Assemblies**.

Temperature:

Operating	0 to +49 degrees C
Non-operating . .	-57 to +68 degrees C

Altitude:

Operating	-100 to 15,000 feet
Non-operating . .	-100 to 40,000 feet
Humidity	0 to 100 percent

1-4.3 **Equipment and Accessories Supplied**. Table 1-2 lists equipment and accessories supplied as part of the wind measuring set, and gives applicable weight and dimensions.

Table 1-2. Wind Measuring Set Equipment and Accessories Supplied

Qty.	Item	Dimensions (Inches)			Weight (lb)
		Width	Height	Depth	
1-4	Wind Direction and Speed Sensor ML-660/FMQ-13(V)	10.69	24.75	5.125	17
~~1-4~~	~~Ruggedized Wind Direction and Speed Sensor ML-660A/FMQ-13(V)~~	10.69	24.75	~~5.125~~	~~17~~
0-16	Digital Display Indicator ID-2408/FMQ-3(V)	19.0	6.97	6.5	11
0-16	Wind Direction and Speed Recorder RO-588/FMQ-13(V)	19.0	21.8	21.8	27

1-4.4 **Related Technical Manuals.** Table 1-3 lists related technical manuals.

Table 1-3. Related Technical Manuals

Publication Number	Publication Title
T.O. 31M1-2FMQ13-2	Maintenance Instruction Manual for Wind Measuring Set AN/FMQ-13(V)
T.O. 31M1-2FMQ13-3	Circuit Diagrams Manual for Wind Measuring Set AN/FMQ-13(V)
T.O. 31M1-2FMQ13-4	Illustrated Parts Breakdown for Wind Measuring Set AN/FMQ-13(V)
T.O. 31M-1-06	Work Unit Code Manual for Wind Measuring Set AN/FMQ-13(V)
T.O. 31M1-2FMQ13-6WC-1	Scheduled Periodic Inspection Work Cards for Wind Measuring Set AN/FMQ-13(V)
T.O. 31S5-4-4019-12	Operator & Commercial Manual, Printer Model ML184 Turbo (Okidata Commercial Manual)

CHAPTER 2

OPERATION

Section I. CONTROLS AND INDICATORS

2-1 INTRODUCTION.

This section describes and illustrates the switches, controls, lamps, displays, and connectors required for operation of the wind measuring set. Review this section completely before performing the operating instructions of Section II.

2-2 CONTROLS AND DISPLAYS/LAMPS.

The following paragraphs cover only those items used by the operator. Items used by maintenance personnel are covered in the instructions for the appropriate maintenance category.

2-2.1 **Indicator**. All operator controls, lamps, switches, and displays for the indicator are described in table 2-1 and illustrated in FIGURE 2-1. Rear panel switches and connectors for the indicator are described in table 2-2 and illustrated in FIGURE 2-2.

2-2.2 **Recorder**. All operator controls, lamps, switches, and displays for the recorder assembly are described in table 2-3 and illustrated in FIGURE 2-3. Rear panel switches and connectors for the recorder assembly are described in table 2-4 and illustrated in FIGURE 2-5. FIGURE 2-4 shows the printer front panel buttons and lamps.

Table 2-1. Indicator, Description of Operator Controls and Displays

Control/Indication	Function
WIND DIRECTION-DEGREES display (7-segment, 3-decimal digit LED display)	Displays wind direction from 0 to 360 degrees to the nearest degree. Wind direction is calculated by vectorially averaging the wind direction values from the displayed sensor over a 2-minute period. Computed directions of 0 and 360 degrees are displayed as 360 degrees. Calm winds are displayed as 000 direction. Update of these 2-minute average values is made every 5 seconds. Display flashes at a 1.0 +/- 0.25 Hz rate until a 2-minute data base is established and when an error is detected by the BIT.
WIND SPEED-KNOTS display (7-segment, 3-digit LED display)	Displays wind speed from 0 to ~~250~~ 99 knots to nearest knot. Wind speed is calculated by vectorially averaging the wind speed averages from the displayed sensor over a 2-minute period. Calm winds are displayed as 000. Update of these 2-minute values is made every 5 seconds. Display flashes at a 1.0 +/- 0.25 Hz rate until a 2-minute data base is established and when an error is detected by the BIT.
GUST-KNOTS display (7-segment, 3-digit LED display)	Displays maximum gusts (to nearest knot) measured during the past 10 minutes. When a gust spread of at least 10 knots has occurred and the 10-minute peak exceeds the current 2-minute average by 5 knots or more, the 10-minute peak wind will be displayed as the gust. Gusts are updated every 5 seconds. When no gusts are present, or the 2-minute wind is calm, the gust display will display all zeroes. Display flashes at a 1.0 +/- 0.25 Hz rate until a 10-minute data base is established and when an error is detected by the BIT.
DIRECTION VARIABILITY-DEGREES (two groups of 7-segment, 3-digit LED displays)	Displays extreme values of wind direction which bracket all wind directions identified during the past 10-minutes. Display is updated every 5 seconds. Display flashes at a 1.0 +/- 0.25 Hz rate until a 10-minute data base is established and when an error is detected by the BIT. When direction variability exceeds 359 degrees the current wind direction value is displayed in both Direction Variability displays as well as the Wind Direction display.
GUST SPREAD-KNOTS display (7-segment, 2 digit LED display)	Displays maximum gust spread over the past minute to the nearest knot. Gust spread is updated every 5 seconds. Display flashes at a 1.0 +/- 0.25 Hz rate until a 1-minute data base is established and when an error is detected by the BIT.

Table 2-1. Indicator, Description of Operator Controls and Displays - CONT

Control/Indication	Function
TIME-HOURS/MINUTES/SECONDS display (two groups of 7-segment, 2-digit LED displays)	Displays real time in hours, minutes, and seconds. Time is set by the SET TIME AND DATE pushbuttons. The selected LED field of the display flashes when a time is being set.
DATE-MONTH/DAY-YEAR display (two groups of 7-segment, 2-digit LED displays)	Displays date in month, day, and year. Date is set by the SET TIME AND DATE pushbuttons. The selected LED field of the display flashes when date is being set.
SET/RUN pushbutton	Selects either set mode or run mode for the TIME AND DATE displays.
FIELD SELECT pushbutton	Pressing the FIELD SELECT pushbutton will cause the HOURS, MINUTES, SECONDS, MONTH, DAY, and YEAR fields of the TIME and DATE display to blink. In the set mode, the blinking field can be changed using the UP or DOWN pushbutton.
UP pushbutton	In the set mode, depressing this pushbutton will cause the displayed time or date to move forward.
DOWN pushbutton	In the set mode, depressing this pushbutton will cause the displayed time or date to move backward.
ACTIVE SENSOR display 7-segment, 1-digit LED display)	Displays the number of the active sensor.
STATUS display (7-segment, 2-digit LED display)	Flashes and displays an error code if the built-in test has failed. Indicates a malfunction in the sensor or indicator, or a communication failure.
STATUS CLEAR pushbutton	Clears the STATUS display. The STATUS display will stop flashing but the error code will stay displayed if fault remains. Also used to enter the STATUS DISPLAY MODE in conjunction with the LAMP TEST pushbutton.
LAMP TEST pushbutton	Pressing the LAMP TEST pushbutton activates all 7-segment displays on the indicator panel. Allows verifying that all segments of 7-segment displays are on. A number 8 is displayed on every display when all segments are activated. Also used to enter the STATUS DISPLAY MODE in conjunction with the STATUS CLEAR pushbutton.

Table 2-1. Indicator, Description of Operator Controls and Displays - CONT

Control/Indication	Function
SENSOR SELECT pushbutton and LED lamps	At the master indicator, pressing one of the SENSOR SELECT pushbuttons simultaneously with the ACTIVE SENSOR-SELECT pushbutton will select the active sensor. Pressing a SENSOR SELECT pushbutton at any indicator, without simultaneously pressing the ACTIVE SENSOR-SELECT pushbutton, will momentarily display wind data from the selected sensor. After 1 minute, the momentary select function will time out and wind data from the active sensor will again be displayed. Depressing the switch before 1 minute has passed will terminate the momentary function. The LED lamp next to each SENSOR SELECT pushbutton is lit when the momentary sampling function is enabled for the sensor.
POWER switch/Circuit Breaker	Provides on/off control of primary power to the indicator. The POWER switch includes a circuit breaker which is tripped by a current overload. If the circuit breaker is tripped, it may be reset by switching to the OFF position and then to the ON position.
TELEPHONE jack	Allows connecting a telephone to provide voice communication among the sensor, indicator, and recorder sites.
ACTIVE SENSOR-SELECT pushbutton	Used in conjunction with the SENSOR SELECT pushbuttons at the master indicator to select the active sensor. Wind data from the active sensor will be displayed on all indicators/ recorders.

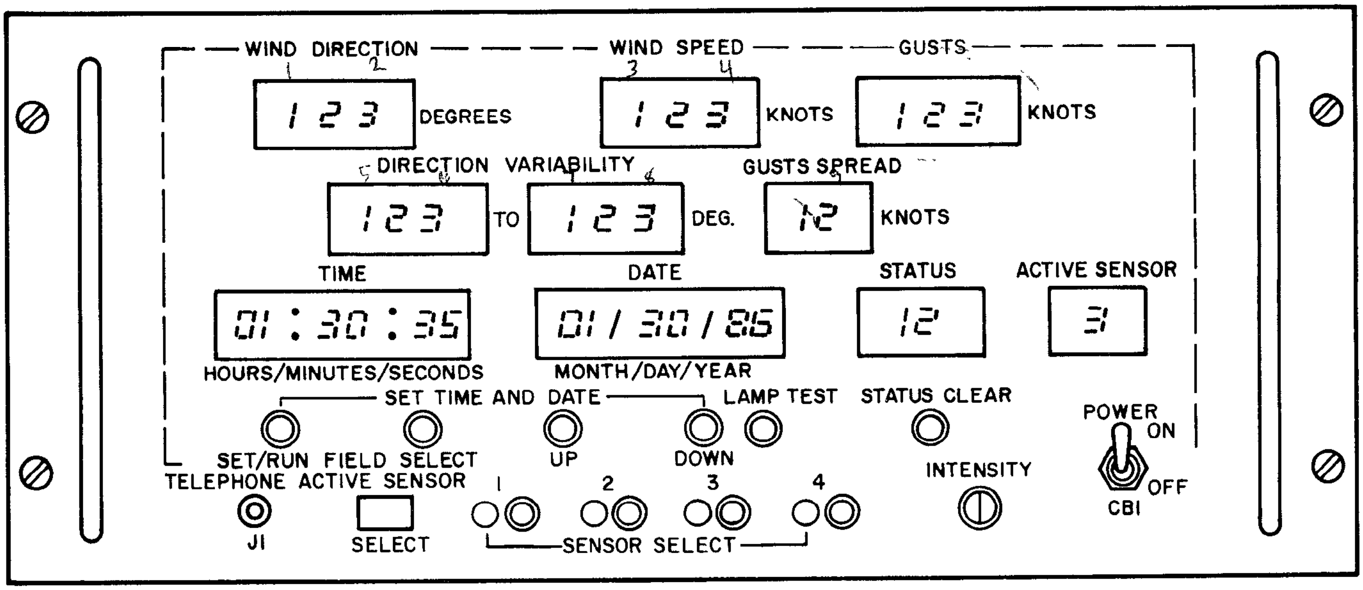


FIGURE 2-1. Indicator-Front Panel Controls, Displays/Lights, Switches, and Displays

Table 2-2. Indicator, Description of Rear Panel Switches and Connectors

Control/Indication	Function
CONFIGURATION switch (SI)	Sets configuration of the local indicator.
MASTER position	Selects the local indicator as the master (only one master per system), providing the ability to designate the active sensor that will be used by all indicators/recorders. The master also manages inter-assembly data communications. There can be only one master per system.
BACKUP position	Selects the local indicator as the backup to assume the functions of the master if the master fails. The backup indicator cannot change the active sensor. There can be only one backup per system.
REGULAR position	Selects the indicator as a regular. The indicator cannot change the active sensor and does not manage inter-assembly communications.
AC POWER connector (J2)	Provides connection of the AC primary power to the indicator.
AWDS connector (A3J4)	Provides connection between the indicator and the AWDS interface.
INTER-ASSEMBLY COMMUNICATIONS connector (J3)	Provides connection between the indicator and the inter-assembly communication channel.

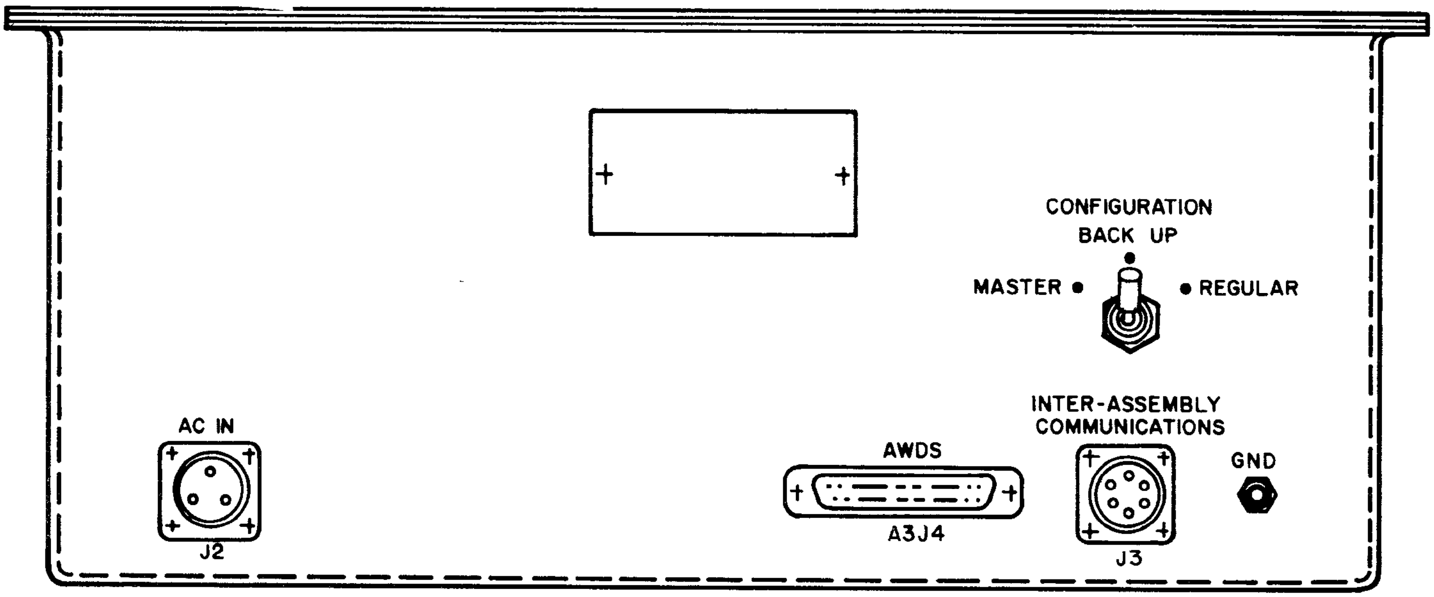


Figure 2-2. Indicator, Rear Panel Switches and Connectors

Table 2-3. Recorder, Description of Operator Controls and Displays

Control/Indication	Function
Display unit:	
WIND DIRECTION-DEGREES display (7-segment, 3-digit LED display)	See indicator. Alternately displays direction of peak wind when a peak-wind (PW) display is selected using the DISPLAY SELECT pushbutton.
WIND SPEED-KNOTS display (7-segment, 3-decimal LED display)	See indicator. Alternately displays speed of peak wind when a peak-wind (PW) display is selected using the DISPLAY SELECT pushbuttons.
GUSTS/PW TYPE-KNOTS (7-segment, 3-decimal LED display)	Displays maximum gust (to nearest knot) when normal mode is selected (see indicator). Alternately displays one of three peak-wind types (P/W TYPE) when a peak-wind mode is selected using the DISPLAY SELECT pushbuttons. The three types are:
Display Reading	Peak Wind Type
	10 — 10-Minute Peak Wind
	60 — 60-Minute Peak Wind
	24 — 24-Hour Peak Wind

Table 2-3. Recorder, Description of Operator Controls and Displays - CONT

Control/Indication	Function
DIRECTION VARIABILITY/ SD DEGREES display (two groups of 7-segment, 3-digit LED displays)	Displays direction variability when normal display mode is selected (see indicator). Alternately displays the standard deviation of wind direction over the latest 10 minutes when a peak-wind mode is selected using the DISPLAY SELECT pushbuttons.
GUST SPREAD-KNOTS display (7-segment, 2-digit LED display)	See indicator.
TIME/PW OCCURRENCE-HOURS/MINUTES/ SECONDS displays (two groups of 7-segment, 2-digit LED displays)	Displays real time in hours, minutes, and seconds. Alternately displays time and peak-wind occurrence when in a peak-wind display mode. Time LED is set by the SET TIME AND DATE pushbuttons. The selected field of the display flashes when time is being set.
DATE-MONTH/DAY/YEAR displays (two groups of 7-segment, 2-digit LED displays)	Displays date in month, day, and year. Date is set by the SET TIME AND DATE pushbuttons. The selected field of the LED display flashes when date is being set.
ACTIVE SENSOR display (7-segment, 1-digit LED display)	Displays the number of the active sensor.
STATUS display (7-segment, 2-digit LED display)	Flashes and displays an error code if built-in test has failed. Indicates a malfunction in the sensor or recorder, or a communication failure.
STATUS CLEAR pushbutton	Clears the STATUS display. The STATUS display will stop flashing but the error code will stay displayed if fault remains. Also used to enter the STATUS DISPLAY MODE in conjunction with the LAMP TEST pushbutton.
LAMP TEST pushbutton	See indicator.
DISPLAY SELECT pushbuttons	Selects the type peak wind (10-minute, 60-minute, or 24-hour) that is displayed. Type selection is confirmed by the GUSTS/PW TYPE display.
NORMAL	When this pushbutton is pressed, all normal wind data are displayed.
PW-10	When this pushbutton is pressed, the peak wind over the past 10-minutes is displayed.

Table 2-3. Recorder, Description of Operator Controls and Displays - CONT

Control/Indication	Function
PW-10	The display format is as follows: **Display** / **Information** DIRECTION — Direction of recorded peak wind SPEED — Speed of recorded peak wind GUST/PW — TYPE10 for 10-minute peak-wind information displayed. TIME/PW OCCURRENCE-(HOURS/MINUTES) — The time of occurrence of the recorded peak wind. DIRECTION VARIABILITY/SD — The standard deviation of the wind direction over the last 10 minutes is displayed in the right display. The left DIRECTION VARIABILITY display is blanked. SECONDS/ MONTH/DAY/ YEAR — These displays are blanked.
PW-60	DIRECTION VARIABILITY - GUST SPREAD, when this pushbutton is pressed, the peak wind over the past 60 minutes is displayed. The display format is the same as the PW-10 mode. The GUST/PW TYPE display is a 60.
PW-24	When this pushbutton is pressed, the peak wind over the past 24 hours is displayed. This display format is the same as the PW-10 mode. The GUST/PW TYPE display is a 24.
POWER switch/circuit breaker	Provides on/off control of primary power to recorder. The POWER switch includes a circuit breaker which is tripped by current overloads. It the circuit breaker is tripped, it may be reset by switching to the OFF position and then to the ON position.
TELEPHONE jack	Allows connecting a telephone to provide voice communication between the sensor site and the indicator/recorder sites.
Audible Alarm	Audible tone sounds when the active sensor is changed from the MASTER indicator.

Table 2-3. Recorder, Description of Operator Controls and Displays - CONT

Control/Indication	Function
ALARM RESET pushbutton	Turns off the audible alarm.
Printer:	
Hard Copy Printout	Provides a hard-copy printout of all displayed wind data plus calculated peak-wind information. Asterisks are printed to the right of invalid data fields when the data base for that parameter is not complete. These correspond to flashing displays for parameters with an incomplete data base.
POWER light	Indicates that the printer is turned on.
SEL button	Pressing this switch after the printer is turned on will put the printer in deselect mode, not communicating with the CPU. To return to select mode, simply press the button again. Pressing this switch will also stop the self test.
SEL light	Works in conjunction with the SEL switch. Lights when the printer is selected and therefore ready to receive data from the CPU. The light is out when the printer is deselected and during a self test.
Top button	To set the top of form, the first printing line, at the current location on the print-head, deselect the printer and press this button. You can also deselect 17.1 cpi printing with this button by holding it down when turning the printer on.
FORM FEED button	To advance the paper to the next top of form, press this button while the printer is deselected.
ALARM light	Lights when paper is out or when there is a motor alarm error (unless you have used this command to disable the alarm). Printing stops until the alarm condition is corrected.
LINE FEED button	Pressing this button while the printer is deselected advances paper one line. It is also used to perform a self test. Press this button while turning.

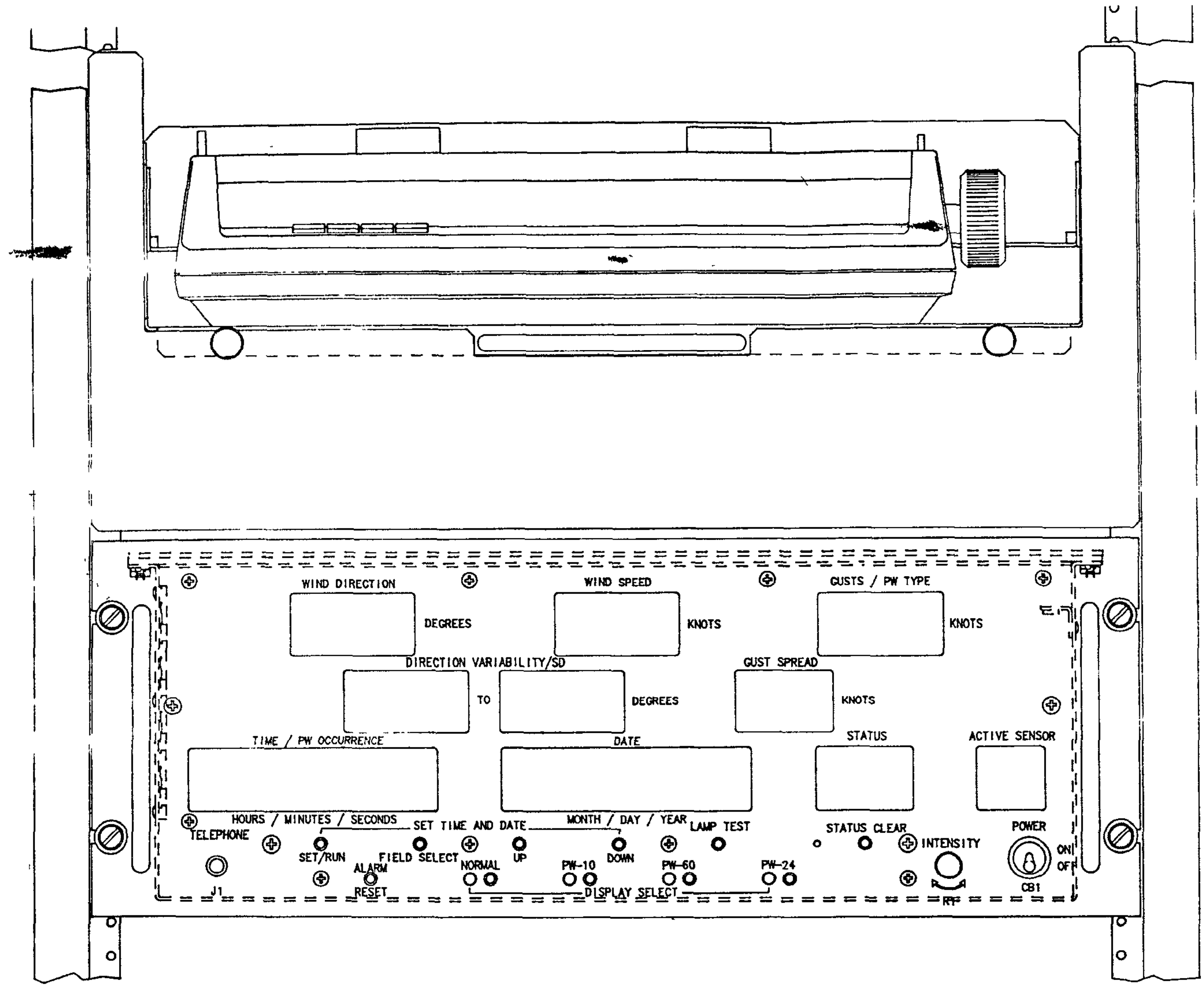


Figure 2-3. Recorder Assembly, Front Panel Controls, Displays/Lights, Switches, and Displays.

Table 2-4. Recorder, Description of Rear Panel Switches and Connectors

Control/Indication	Function
Display unit:	
CONFIGURATION switch (SI)	Sets configuration of the local recorder.
MASTER position	Selects the local recorder as the master (only one master per system). NOTE: The recorder cannot select the active sensor and therefore should not be selected as master in a multi-sensor system. The master also manages inter-assembly data communications. There can only be one master per system.
BACK UP position	Selects the local recorder as backup to assume the communication functions of the master if the master fails. Also used to enter the STATUS DISPLAY MODE. The backup assembly cannot change the active sensor. There can be only one backup assembly per system.
REGULAR position	Selects the recorder as a regular. The recorder cannot change the active sensor and does not manage inter-assembly communications.
AC POWER connector (J4)	Provides connection of primary power to POWER connector on the printer subassembly.
AC IN connector (J2)	Provides connection of AC primary power to the printer subassembly.
PRINTER connector (A3J3)	Provides connection to PRINTER connector on the printer subassembly.
AWDS connector (A3J4)	Provides connection between the recorder and the AWDS interface.
INTER-ASSEMBLY COMMUNICATIONS connector (J3)	Provides connection between the Communications connector recorder and the inter-assembly channel.
Printer:	
POWER connector	Provides connection of the primary power from the AC POWER (J4) connector on the display unit.
PRINTER INTERFACE connector	Provides connection for the PRINTER connector (A3J3) on the display unit.

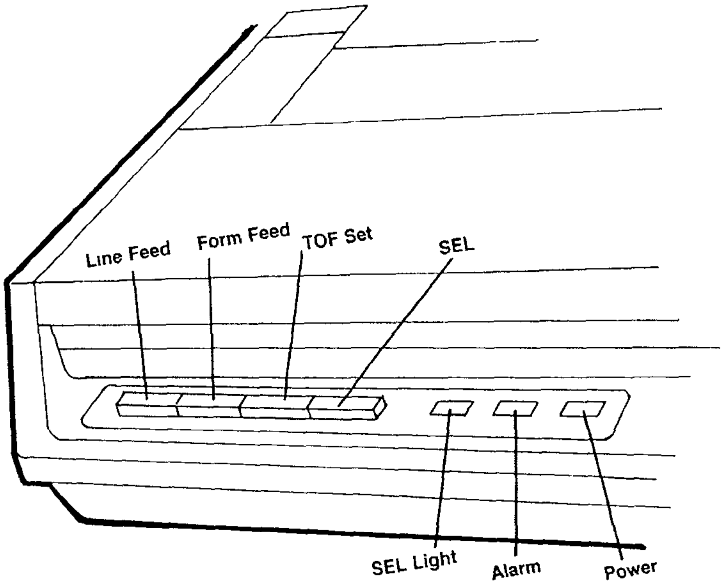


FIGURE 2-4. Printer Front Panel Buttons and Lights

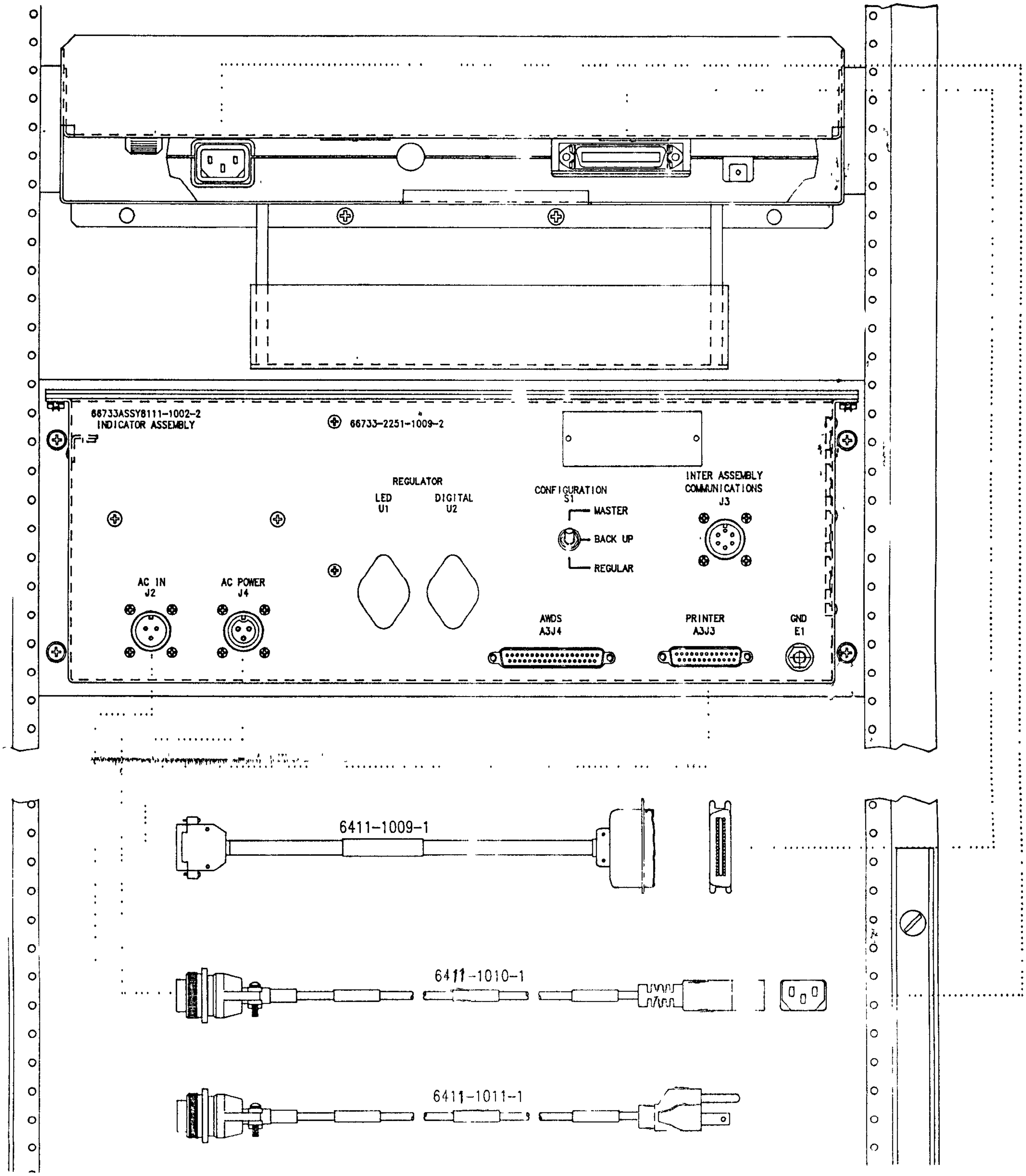


FIGURE 2-5. Recorder - Rear Panel Switches and Connectors
(Shown with associated cables. View shows typical rack-mounted application.)

Section II. OPERATING INSTRUCTIONS

2-3 PRELIMINARY.

Perform the following procedure at the start of each operating period.

a. Verify that all indicator, recorder, and sensor assemblies are turned on.

NOTE

Displays will flash until complete data base is established for the parameter. All displays should stop flashing 10 minutes after the master is initially turned on. An error code of 04 is normal for the first 24 hours of operation. An error code of 06 (04 + 02) will be displayed if any sensor does not have power.

b. Adjust the respective INTENSITY control for desired brightness of indicator and recorder front panel displays.

c. Clear any initial error code by depressing the STATUS CLEAR pushbutton.

d. Before continuing with step e, allow time for the displays to stabilize (displays stop flashing). Displays flash until complete data base is established for that parameter. Maintenance may not be required.

e. Verify that no error code is displayed on the STATUS display of each indicator/recorder. A code of 04 is normal during the first 24 hours of operation. If a hardware fault error code is displayed or the STATUS display flashes, maintenance is required.

2-4 SETTING TIME AND DATES.

Set time and date on each indicator or recorder as follows:

NOTE

When the SET/RUN is depressed initially, HOURS is displayed on the TIME display. The time or date selected by the FIELD SELECT pushbutton will flash the 2-digit LED field selected. Each time the UP/DOWN pushbuttons are depressed, the 2-digit LED field selected will increment by one (up) or decrement by one (down).

a. Set the SET/RUN pushbutton to select the set mode. This is indicated by flashing of the TIME display.

b. If HOURS is not displayed on the TIME display, continue pressing the FIELD SELECT pushbutton until HOURS field of the TIME display flashes.

c. Use the UP and DOWN pushbuttons to enter the desired time in hours on the TIME display.

d. Use the FIELD SELECT pushbutton to select the MINUTES field of the TIME display.

e. Use the UP and DOWN pushbuttons to enter the desired time in minutes on the TIME display.

f. Use the FIELD SELECT pushbutton to select the SECONDS field of the TIME display.

g. Use the UP and DOWN pushbuttons to enter the desired time in seconds on the TIME display.

h. Use the FIELD SELECT pushbutton to select the MONTH field of the DATE display.

i. Use the UP and DOWN pushbuttons to enter the desired month on the DATE display.

j. Use the FIELD SELECT pushbutton to select the DAY field of the DATE display.

k. Use the UP and DOWN pushbuttons to enter the desired day on the DATE display.

l. Use the FIELD SELECT pushbutton to select the YEAR field of the DATE display.

m. Use the UP and DOWN pushbuttons to enter the desired year on the DATE display.

n. Use the SET/RUN pushbutton to exit the set mode. The TIME and DATE displays will update automatically.

2-5 NORMAL OPERATION.

2-5.1 **Displaying Wind Data From Active Sensor**. Horizontal wind direction, wind speed, and wind gust data from the active sensor is continuously displayed on all system indicators and recorders. Weather data displayed includes:

Wind Data	Parameter
Wind Direction	0 to 360 degrees
Wind Speed	0 to ~~150~~ 99 knots
Gusts	Displays maximum wind gusts occurring within the past 10 minutes. The recorder can also display peak wind occurring within the past 10 minutes, 1 hour, or 24 hours.
Direction Variability	Displays the two extreme values of wind direction that bracket all direction identified during the last 10 minutes of system operation (in a clockwise direction).
Gust Spread	Maximum gust spread over the past minute is calculated.

2-5.2 **Displaying Wind Data From Sensor Other Than Active Sensor**. Wind data from a sensor other than the active sensor can be momentarily displayed at the local indicator. Proceed as follows:

a. Press the SENSOR SELECT pushbutton for the sensor whose wind information is to be displayed without simultaneously pressing the ACTIVE SENSOR-SELECT pushbutton. The corresponding LED lamp should be lit.

b. Wind data from the selected sensor will be momentarily displayed for a period of 1 minute.

c. Pressing the same SENSOR SELECT pushbutton will cause the display to revert back to the active sensor. The corresponding LED lamp will turn off.

2-5.3 **Displaying Peak Wind On Recorder**. The recorder has the capability of displaying the peak wind measured during intervals of 10 minutes, 60 minutes, and 24 hours. The direction of the peak wind is given by the DIRECTION display. The speed of the peak wind is given by the SPEED display. The type of peak wind is given by the GUST/PW TYPE display (i.e. 10 for 10-minute peak winds, 60 for 60-minute peak winds, and 24 for 24-hour peak winds). The HOUR and MINUTE displays give the time of occurrence of the peak wind. The standard deviation of the wind direction is given by the right DIRECTION VARIABILITY/SD display. All other displays are blanked except for the STATUS and ACTIVE SENSOR displays.

2-5.4 **Fault Monitoring**. The result of each built-in-test (BIT) is reported using a two-level display scheme. The first level is the normal operating display mode. The second level is called the STATUS DISPLAY MODE. The status information available in these two display modes is described below.

2-5.4.1 **Normal Display Mode**. The normal display mode provides wind, time, date, active sensor, and status data. The STATUS display is a two-digit display that provides a summary of the status of the various BITs. This provides a "general status" indication for all the BITs running on the specific indicator or recorder assembly as well as the BITs running on each sensor. A status code of 00 indicates normal operation and that all wind data bases are complete and valid. When a fault is detected a non-zero code will be displayed by the two STATUS LEDs. The STATUS displays will flash when a fault is detected. These general status codes are read separately from the left LED and right LED. Table 2-5 provides the codes for the left LED of the STATUS display. Table 2-6 provides the codes for the right LED of the STATUS display.

2-5.4.2 **Status Display Mode**. The second display level is called the STATUS DISPLAY MODE. This display mode is entered by holding the LAMP TEST pushbutton depressed, then pressing the STATUS CLEAR pushbutton. This display mode can be distinguished by the presence of flashing zeros in the time and date display windows. The middle LEDs of the WIND DIRECTION, WIND SPEED, GUSTS, and DIRECTION VARIABILITY are blanked, along with the left LED of the GUST AND GUST SPREAD LEDs. FIGURE 2-6 shows the assignment of the LED displays in the STATUS DISPLAY MODE. The WIND DIRECTION AND WIND SPEED displays provide the status of the BITs running on the indicator/recorder assembly. The DIRECTION VARIABILITY and GUST SPREAD displays provide the status of the BITs running on the sensors. The SENSOR SELECT pushbuttons are used to select the sensor of interest. Sensor #1 is selected by default upon entering the STATUS DISPLAY MODE as indicated by the #1 LED being lit.

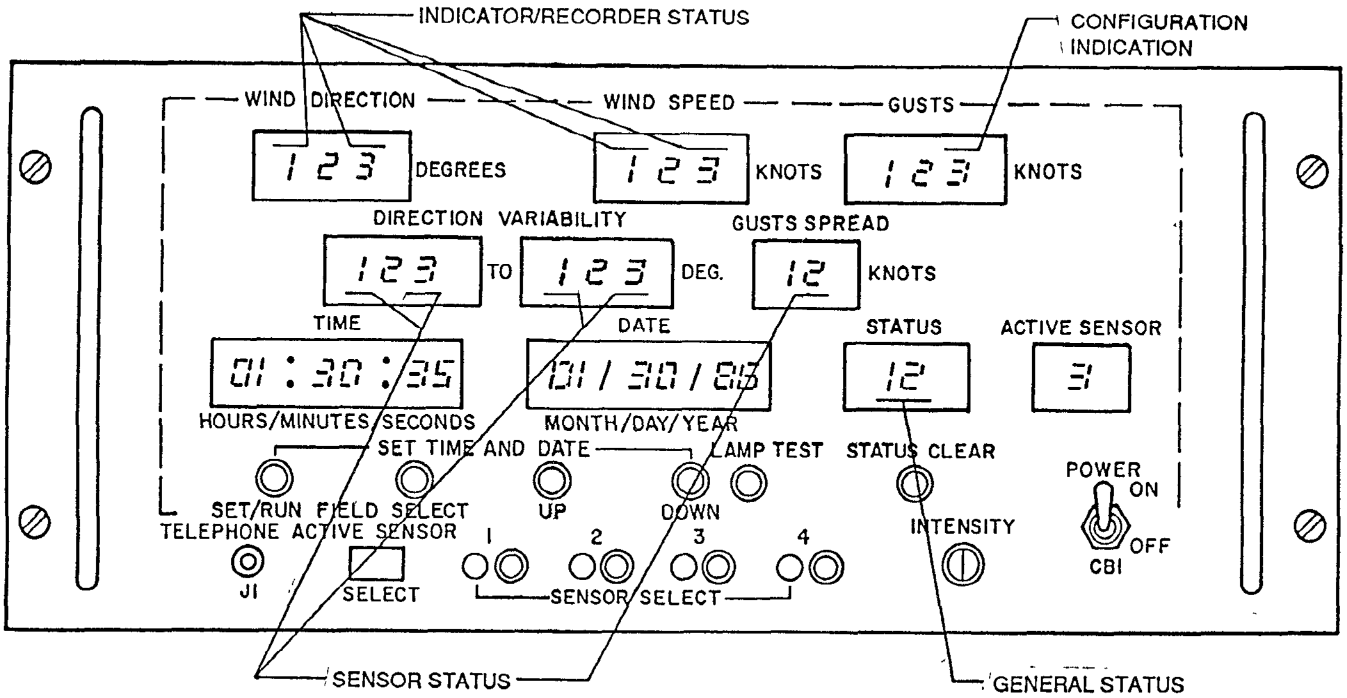


FIGURE 2-6. Error Code Display

2-5.4.3 **Status Codes**. The status of each of the eleven BITs running on the indicator/recorder and the twelve tests running on each sensor are grouped into sets of three and displayed as binary octal codes. This means they are represented by a 3-bit binary count. This means multiple errors within the same group sum to make a combined error code. Each group of codes has been assigned an LED display position and is referenced by a CODE GROUP number as shown in FIGURE 2-7. Tables 2-8 through 2-16 provide the definition of each error code designated by code group number and display name. The CONFIGURATION INDICATION display reports the status of the assembly configuration using the code of 1, 2, and 3 for MASTER, BACKUP, and REGULAR modes, respectively.

2-5.4.4 **Error Code Acknowledgement**. When an error is detected, the two LEDs of the STATUS display will flash and display an error code. The error is acknowledged by pressing the STATUS CLEAR pushbutton. This will cause the display to stop flashing until a new error is detected. The original error code will continue to be displayed as long as the error condition exists. The error code will clear once the error condition has been removed. If an error condition exists only momentarily the error code will clear as soon as the STATUS CLEAR pushbutton is pressed.

NOTE

Pressing the STATUS CLEAR pushbutton while holding the LAMP TEST pushbutton to enter or exit the STATUS DISPLAY MODE will not cause the error code to clear.

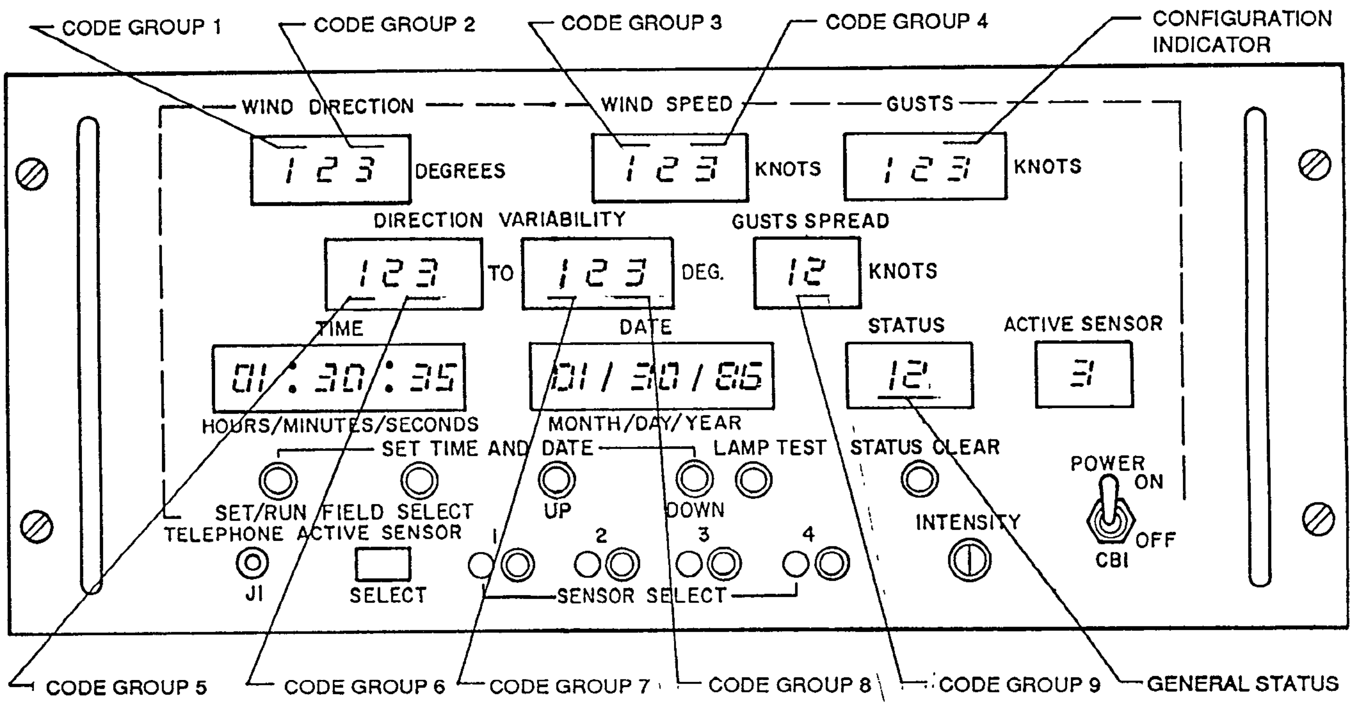


FIGURE 2-7. Error Code Groups (See tables 2-5 to 2-15 for Error Code explanations)

2-5.4.5 **Nominal Status Codes**. Periodically observe the STATUS display on all indicators and recorders. If the STATUS display is flashing, press the STATUS CLEAR pushbutton and observe whether the error code remains unchanged. If the error code is still displayed on the STATUS display, maintenance may be required. A status code of 04 does not require maintenance. A status code of 04 indicates that a data base recovery operation is in process. This will occur at power-up and after any fault that would affect the accuracy of the displayed wind information. There are two types of data base recovery operations: (1) recovery of the 10-minute data base (short-term recovery) and (2) recovery of the complete 24-hour peak-wind data base (long-term recovery). A momentary loss of communications (less than 60 seconds) will cause a recovery of the 10-minute data base. Any detected equipment failure or loss of communications for more than 60 seconds will cause a long-term recovery.

2-5.5 **Resetting Recorder Alarm**. The recorder's audible alarm sounds whenever the active sensor is changed at the MASTER indicator. Press the ALARM RESET pushbutton on the recorder front panel to reset the alarm.

2-5.6 **Printer Paper Supply**. Install paper supply as follows (refer to FIGURE 2-8):

a. Remove the paper access cover.

b. Place fan fold paper in the paper supply shelf.

c. Remove printer access cover and lift the paper bail.

d. Open the paper lever located on top right of the printer just above the platen knob. (The paper lever must remain open for sprocket fed paper.)

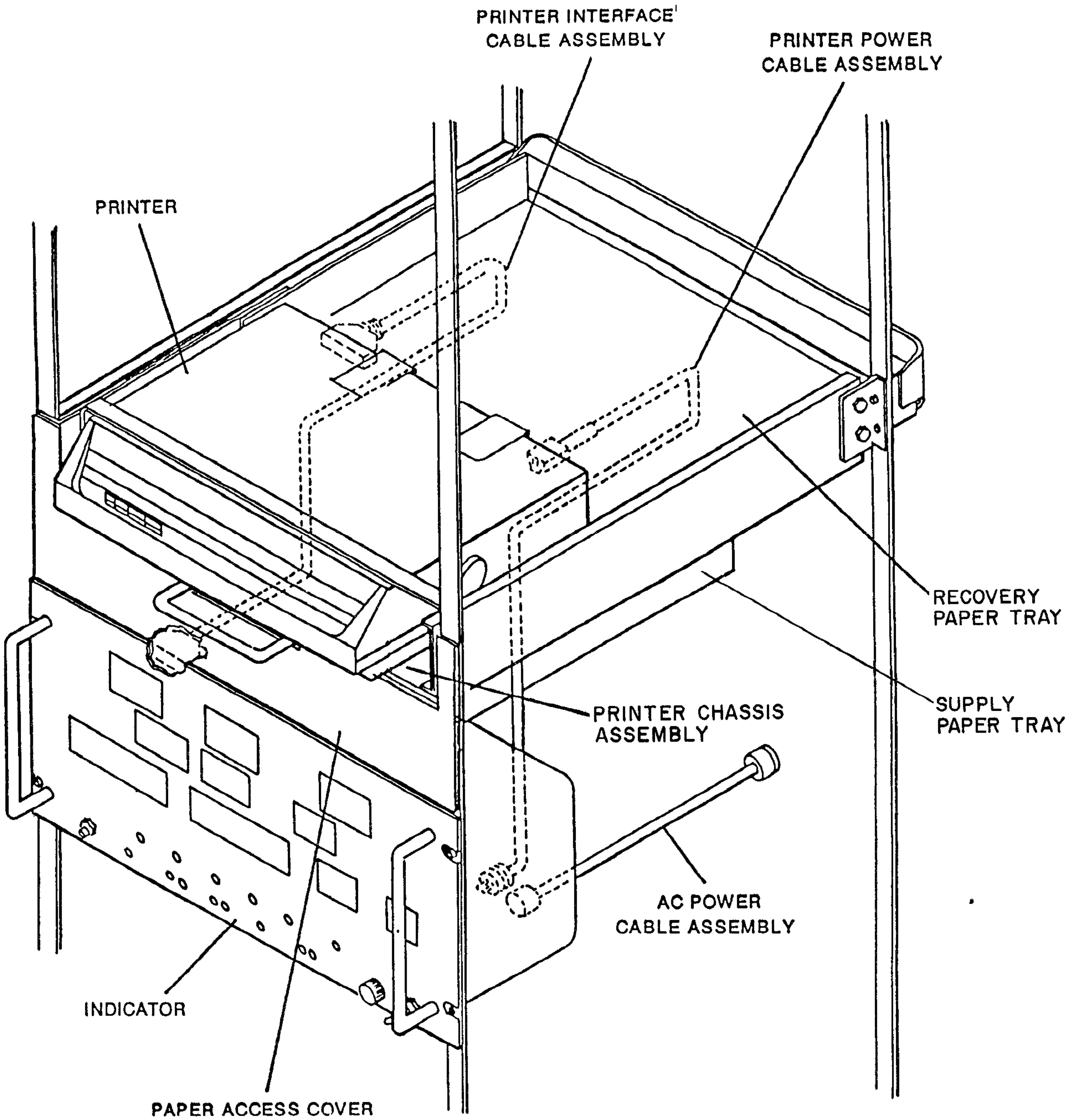


FIGURE 2-8. Printer Paper Serving On Wind Direction and Speed Recorder RO-588/FMQ-13(V)

e. Route the paper up through the bottom of the printer through the printer access slot.

f. Slide the paper up until it appears in front of the platen.

g. Align the holes on either side of the paper with the corresponding pins of the adjustable feeds on either side of the carriage.

h. Lower the paper bail.

i. Use the platen knob to advance the paper to the first printing line at the top of the second page.

j. Replace the printer access cover routing the paper through the slot in the cover.

k. Use the platen knob to advance the paper until a minimum of two pages are resting in the paper recovery tray behind the printer.

CAUTION

When installing the paper access cover onto the printer chassis assembly the grommets of the latches must be completely inserted into the latch holes of the printer chassis assembly. Be certain that the back of the access cover butts up against the flange of the printer chassis assembly before pushing the plunger in to expand the grommet. Failure to do so can cause the latch grommet to be damaged creating an ineffective latch.

l. Install the paper access cover onto the printer chassis assembly as shown in FIGURE 2-8. This is done by pulling the plunger out, positioning the paper access panel to engage the grommets into the latch holes, and pushing the plunger in to expand the latch.

m. Use the pushbuttons on the front of the printer to deselect the printer and form feed a minimum of two pages into the paper recovery tray. This will allow the paper to continue to fold into the recovery tray as more paper is used.

n. Place the printer back on-line by depressing the SELECT pushbutton on the printer.

o. Clear the status display by depressing the STATUS CLEAR pushbutton on the indicator to clear the error codes generated while changing the paper.

2-5.7 **Operating the Printer**. Refer to the printer operation manual for operating instructions.

2-6 **SHUTDOWN**. Turn off all sensors, indicators, and recorders by placing the POWER switch on respective assembly in the OFF position.

Table 2-5. General Status Codes, STATUS Display-Left Digit

Display Code Number	Indicated Status
0	No Errors
1	Processor PCBA fault. Failure of one or more of the following tests: (1) CPU Test, (2) ROM Test, (3) RAM Test, or (4) Inter-Assembly Communications Port Loop Test.
2	Sensor Error - Any error report from the sensor
3	Combination of codes 1 and 2
4	Loss of Master
5	Combination of codes 1 and 4
6	Combination of codes 2 and 4
7	Combination of codes 1, 2, and 4

Table 2-6. General Status Codes, STATUS Display-Right Digit

Display Code Number	Indicated Status
0	No Errors
1	Printer Error (Receiver Only)
2	Inter-Assembly Communications Error. Failure of one or more of the following tests: (1) Communications 5-second Time-Out, (2) CRC-16 Error, (3) Carrier Time-Out, and/or (4) No Sensor Response.
3	Combination of codes 1 and 2
4	Recovery in Progress
5	Combination of codes 1 and 4
6	Combination of codes 2 and 4
7	Combination of codes 1, 2, and 4

Table 2-7. Status Display Mode Codes, Indicator/Recorder Status Word
WIND DIRECTION Display-Left Digit (Code Group 1)

Display Code Number	Indicated Status
0	No Errors
1	Inter-Assembly Communications Loop Test Failure
2	Inter-Assembly 5-second Communications Time-Out Error
3	Combination of codes 1 and 2
4	Inter-Assembly Carrier Time-Out Error
5	Combination of codes 1 and 4
6	Combination of codes 2 and 4
7	Combination of codes 1, 2, and 4

Table 2-8. Status Display Mode Codes, Indicator/Recorder Status Word
WIND DIRECTION Display-Right Digit (Code Group 2)

Display Code Number	Indicated Status
0	No Errors
1	CPU Test Failed
2	ROM Test Failed
3	Combination of codes 1 and 2
4	RAM Test Failed
5	Combination of codes 1 and 3
6	Combination of codes 2 and 4
7	Combination of codes 1, 2, and 4

Table 2-9. Status Display Mode Codes, Indicator/Recorder Status Word
WIND SPEED Display-Left Digit (Code Group 3)

Display Code Number	Indicated Status
0	No Errors
1	Printer Paper Out
2	Printer Off-Line
3	Combination of codes 1 and 2
4	Printer Fault
5	Combination of codes 1 and 4
6	Combination of codes 2 and 4
7	Combination of codes 1, 2, and 4

Table 2-10. Status Display Mode Codes, Indicator/Recorder Status Word
WIND SPEED Display-Right Digit (Code Group 4)

Display Code Number	Indicated Status
0	No Errors
1	AWDS Loop Test Failed
2	N/A
3	N/A
4	Loss of Master
5	Combination of codes 1 and 4
6	N/A
7	N/A

Table 2-11. Status Display Mode Codes, Sensor Status Word DIRECTION VARIABILITY Left Display-Left Digit (Code Group 5)

Display Code Number	Indicated Status
0	No Errors
1	Multiple Reset Error
2	Counter Test Failed
3	Combination of codes 1 and 2
4	Inter-Assembly Loop Test Failed
5	Combination of codes 1 and 4
6	Combination of codes 2 and 4
7	Combination of codes 1, 2, and 4

Table 2-12. Status Display Mode Codes, Sensor Status Word DIRECTION VARIABILITY Left Display-Right Digit (Code Group 6)

Display Code Number	Indicated Status
0	No Errors
1	CPU Test Failed
2	ROM Test Failed
3	Combination of codes 1 and 2
4	RAM Test Failed
5	Combination of codes 1 and 4
6	Combination of codes 2 and 4
7	Combination of codes 1, 2, and 4

Table 2-13. Status Display Mode Codes, Sensor Status Word
DIRECTION VARIABILITY Right Display-Left Digit (Code Group 7)

Display Code Number	Indicated Status
0	No Errors
1	Out of Range Error
2	Pressure Sensor Test Failed
3	Combination of codes 1 and 2
4	Power Supply Test Failed
5	Combination of codes 1 and 4
6	Combination of codes 2 and 4
7	Combination of codes 1, 2, and 4

Table 2-14. Status Display Mode Codes, Sensor Status Word
DIRECTION VARIABILITY Right Display-Right Digit (Code Group 8)

Display Code Number	Indicated Status
0	No Errors
1	A/D Test Failed
2	Element Driver Test Failed
3	Combination of codes 1 and 2
4	Temperature Sensor Test Failed
5	Combination of codes 1 and 4
6	Combination of codes 2 and 4
7	Combination of codes 1, 2, and 4

Table 2-15. Status Display Mode Codes, Sensor Status Word
GUST SPREAD Display - Right Digit (Code Group 9)

Display Code Number	Indicated Status
0	No Errors
1	Long Recovery in Process
2	No Sensor Response
3	Combination of Codes 1 and 2
4	CRC 16 Error
5	Combination of codes 1 and 4
6	Combination of codes 2 and 4
7	Combination of codes 1, 2, and 4

Section III. EMERGENCY OPERATION

There are no emergency operating procedures for the wind measuring set.

CHAPTER 3

THEORY OF OPERATION

Section I. FUNCTIONAL SYSTEM(S)

3-1 INTRODUCTION.

This section provides functional descriptions of the major assemblies and functions thereof comprising the wind measuring set. Narrative descriptions are supported by block diagrams. Refer to Section II for detailed functional descriptions of each unique printed circuit board assembly (PCBA). The following is a description of the communication protocol used by all the assemblies.

3-1.1 **Inter-Assembly Communications Overview**. All the assemblies of the wind measuring set communicate via an inter-assembly communications network consisting of cabling between the separate units over which serial digital information is transmitted. This network forms a broadcast bus, which means information from one assembly will be broadcast to all other assemblies simultaneously over the same physical link. The protocol, which governs access to the network, incorporates a master control unit. This master unit, which is switch selectable and can be either an indicator or recorder, polls the sensors for the latest data every 5 seconds. When a sensor is polled, it transmits the latest 5-second wind sample three times. This gives each receiving assembly three chances to acquire the data. Each assembly processes the data as soon as it is received. If the master unit does not receive a response or receives a corrupted response, it will repoll the sensor as many as two more times before moving on to the next sensor.

3-1.2 **Inter-Assembly Communication Protocol**. Inter-assembly communication is accomplished using a shared multi-drop serial data link configuration. Data transmission is accomplished using Bell 202 compatible FSK techniques. Asynchronous serial data transmissions occur at a 1200 baud rate over a physical network comprised of a single pair of wires (two wires) connected to each assembly. Each character frame consists of one start bit, one stop bit, and eight data bits with no parity generation. This signal format is used to transmit messages between the assemblies. The general protocol uses a central control element to govern the use of the network. This controller is referred to as the MASTER assembly. The MASTER assembly has the responsibility of polling the sensors every 5 seconds. There is only one MASTER assembly allowed in a system. A polling session starts every 5 seconds and commences with a poll request to sensor number 1.

NOTE

> The sensor identification number (ID#) is established by jumper settings in the sensor assembly. Sensor ID#s must be assigned starting with ID#-1 and running consecutively up to a maximum of four for inter-assembly communications to work properly.

When sensor #1 receives the poll request, it transmits the latest 5-second average X and Y wind values three times. This poll response and all inter-assembly transmissions are broadcast over the network to all assemblies to receive. After the MASTER receives the poll response from sensor #1, it polls sensor #2. This process continues until each sensor in the system is polled. The "number of sensors" (NSNR) jumpers on the indicator/recorder assembly establish how many sensors will be polled by the MASTER. There are several negative acknowledge and redundancy schemes used in the protocol which is described in detail in the following paragraphs.

3-1.2.1 **Description of Modes of Operation.** The inter-assembly CPC provides serial I/O data processing, sensor polling control, and message error checking to assure reliable communications. There are three modes of operation which are selected by a switch setting on the back of each assembly. These modes are referred to as Master, Backup, and Regular The function of each mode is described in detail in Paragraphs 3-1.2.1.1 through 3-1.2.1.3.

To summarize these functions:

a An assembly in Master mode polls the sensors for data every 5 seconds and processes the responses.

b. An assembly in Regular mode receives all communications and processes wind data.

c. An assembly in Backup mode will function as if in Regular mode unless the master quits polling, in which case the backup assembly will start polling. This arrangement provides redundancy of the system control element.

3-1.2 1.1 **Description of Master Mode.** Each system will have one, and only one, assembly designated to operate in Master mode. In this mode, the assembly is the primary sensor polling device. No other assembly can poll the sensors as long as the Master assembly is operating properly. The polling sequence is described in paragraph 3-1.2.1.1.1. The only other unique function performed by the Master assembly is its interaction with the designated Backup assembly which is described in paragraph 3-1.2.1.3. All the other inter-assembly communication functions are a part of Regular mode operation described in paragraph 3-1.2.1.2.

3-1.2.1.1 1 **Sensor Polling Sequence.** The Master assembly will poll each sensor in the system every 5 seconds. If there is no response from a sensor or if the response is corrupted, the Master will repoll the sensor at fault. A second repoll will be sent if no satisfactory response is received. If there is still no satisfactory response from the sensor, the Master assembly will indicate an error condition and will proceed with polling the other sensors of the system. A polling cycle is comprised of a polling session of each sensor in the system. A polling session consists of a poll of a single sensor and up to two repolls of the same sensor. If a sensor fails to satisfactorily respond through two consecutive polling cycles, the Master assembly will subsequently poll the faulty sensor only once each cycle until a good response is received. At the point, the same repolling strategy will be used again until two consecutive faulty responses are received over two consecutive polling cycles.

3-1 2.1.2 **Description of Regular Mode.** An assembly in Regular mode listens to all inter-assembly communications, tracking the poll/response sequence and extracting wind data and system status information Each inter-assembly message has a poll count number. This modulo 16 count is generated by the master assembly and is incorporated into the sensor response. Each assembly uses the count to determine if any messages have been missed and how many. The count is also used to determine that a retransmitted message has already been received and processed. If the sequence is broken, an error code will be displayed. If no messages are received over a period of 5 seconds, the assembly will indicate a timeout error code.

3-1.2.1.3 **Description of Backup Mode.** One, and only one, assembly in each system should be placed in Backup mode. This assembly will function as a regular assembly until two consecutive 5-

second timeout errors occur. At this point, the Backup unit will assume the polling responsibilities of the Master assembly. The Opcodes used by the Backup assembly for polling are different from the Master Opcodes. These codes can be detected by all assemblies, thereby informing them that the Backup assembly is operating as Master. The detection of the backup Opcode causes an error code to be displayed on all operating assemblies. If the Master assembly starts functioning or if another assembly is enabled to be Master, it will listen for inter-assembly communication. Upon detection of the backup Opcode, the Master will wait until the current polling cycle is complete, at which time a "master takeover" command will be issued. This informs the backup unit that a Master unit is in control and the Backup will halt any further polling and will revert to standby operation.

NOTE

The Backup unit cannot be used to select the active sensor. This function is reserved for the Master unit only.

3-1.2.2 **Inter-Assembly Communication Message Format**. The protocol uses message packets to exchange information between assemblies. Each message is framed using standard ASCII control character pairs (DLE STX and DLE ETX). Each packet has a 16-bit cyclic redundancy check (CRC) number affixed to the end of the message for error checking. A sample message packet is shown here:

DLE, STX, MESSAGE, DLE, ETX, CRC, CRC

The control pair DLE, STX signifies the start of a transmission. DLE, ETX signifies the end of a transmission. The MESSAGE section is variable in length. The information contained in the MESSAGE section is detailed below.

3-1.2.2.1 **Inter-Assembly Communication Message Opcode**. Each message contains an Opcode as well as data. The Opcode character has eight bits of which only four are used for the actual operation code. The other four bits are used for identification purposes. Two bits are used to indicate the active sensor number and two bits are used for the sensor ID number which identifies the sensor that the message is sent to or received from. These bit assignments are provided in table 3-1. The format of the Opcode character and a list of the codes are provided in table 3-2.

Table 3-1. Inter-Assembly Opcode Bit Assignments

BIT#	Description
0	OPCODE BIT 0
1	OPCODE BIT 1
2	OPCODE BIT 2
3	BACK UP OPCODE BIT
4	SENSOR ID BIT 0
5	SENSOR ID BIT 1
6	ACTIVE SENSOR ID BIT 0
7	ACTIVE SENSOR ID BIT 1

Table 3-2. Inter-Assembly Opcodes

Code	Description
0	Illegal Code
1	Poll
2	Repoll
3	Poll Response
4	Repoll Response
5	(unassigned)
6	(unassigned)
7	(unassigned)
8	(unassigned)
9	Backup Poll
A	Backup Repoll
B	Backup Repoll
C	Backup Repoll Response
D	(unassigned)
E	(unassigned)
F	Master Take Over

3-1.2.2.2 **Inter-Assembly Communication Message Data**. The information contained in the data field of a poll request sent by the Master assembly is a modulo 16 poll count used by all the assemblies to track the sequence of poll requests and poll responses between the Master and the sensors. Use of the poll count is described further in paragraph 3-1.2.1.2.

A sensor response data field consists of wind data, sensor status, and an echo of the poll count received with the poll request from the Master assembly. Normally, four bytes of wind data are transmitted. However, the wind and status data are transmitted in 8-bit hexadecimal format as opposed to ASCII code. If the data value is the same as a DLE, then a second DLE character is sent to indicate that the first DLE was a data value and not a control character (e.g. DLE, ETX or DLE, STX). This provides a "transparency" of a DLE value occurring in the data field. In worst case this could produce eight bytes of wind data values if all four wind values were DLEs (10 HEX).

3-1.2.2.3 **Inter-Assembly Communication Message Timing**. Communications are carried out using 1200 baud as the transmit and receive rate. This works out to be 8.33 milliseconds/character. Using this rate, a poll request takes 66.64 milliseconds to send the following eight bytes of information:

DLE, STX, OPCODE, POLLCNT, DLE, ETX, CRC, CRC

The data message in the poll request is the poll count (POLLCNT), which is a modulo 16 count used to track message sequencing.

A poll response from the sensor will nominally require 108.3 milliseconds to send the following message:

DLE, STX, OPCODE, POLLCNT, WD, WD, WD, WD, STATUS, DLE, ETX, CRC, CRC

WD indicates one byte of wind data. The worst case time which corresponds to eight bytes of wind data (four extra DLE characters) is equal to 150 milliseconds. Worst Case Poll Response:

Each wind data field requires a DLE to follow

DLE, ETX, OPCODE, POLLCNT, DATA1...DATA8,
STAT1, STAT2, DLE, STX, CRC, CRC

18 Bytes (8.33 ms/byte) - 150 ms

An example poll request formatted in hexadecimal format would appear as:

10,02,41,05,10,03,49,FC

The poll starts with a DLE, STX (10,02). The 41 is the opcode. The 4 decodes as a sensor ID# of 0 (sensor number 1) and the active sensor designator is set for sensor number 2. The 1 decodes as a poll opcode. The 05 is the poll count. The message ends with a DLE, STX (10,03) followed by a 16 bit CRC of 49,FC.

The poll response would be:

10,02,43,05,16,00,38,00,00,00,10,03,05,D4

The response starts with a DLE, STX. The 43 contains the same sensor ID and active sensor designator with opcode for a poll response (3). The poll count of 05 is echoed in the response. The wind data consists of the X value of 16,00 and the Y value of 38,00. The status shows no faults (00,00). The message terminates with a DLE, ETX pair followed by a CRC16 of 05, D4.

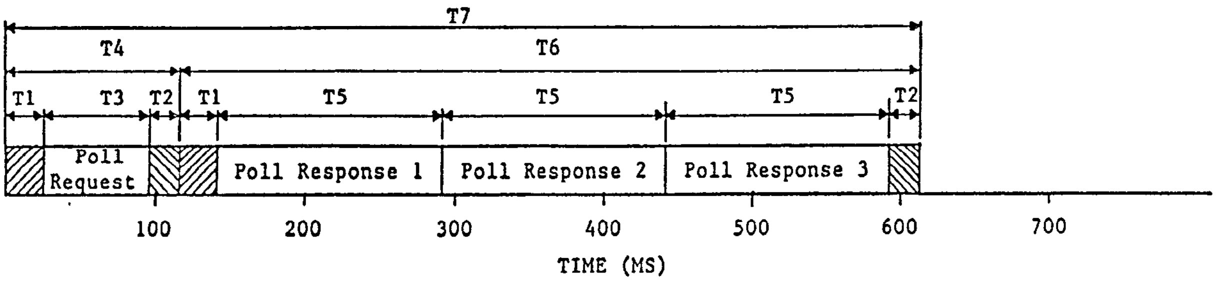
A timing diagram of each component of a poll request and poll response, as well as a complete poll session for four sensors, is shown in FIGURE 3-1. This timing diagram uses the worst case time of 150 ms for the poll response and the maximum latency periods for the carrier detect off-to-on and on-to-off transition.

3-2 SENSOR BLOCK DIAGRAM DESCRIPTIONS.

Paragraph 3-2.1 provides an overall functional description of the sensor. This is followed by block diagram descriptions of the element driver function, measurement function, temperature circuit, barometric pressure circuit, control/status function, Central Processing Unit (CPU) function, inter-assembly communications function, and power supply and distribution circuits.

3-2.1 **Sensor Overall Block Diagram Description**. (See FIGURE 3-2.) The purpose of the sensor is to measure and report wind speed and wind direction. FIGURE 3-2 gives an overview of the functional blocks of the sensor. The sensor uses hot-film technology to sense air flow. The sensing elements consist of two orthogonal thick-film platinum element pairs surrounded by a protective cage. The elements are maintained approximately 100 degrees C above ambient temperature by the element driver circuit. As the wind blows, an increasing amount of energy is required to maintain the elements at the elevated temperature. The energy required to maintain a constant temperature provides a measure of wind speed.

POLLING TIMING



T1 - Carrier Detect Off-On Delay - 25 MS
T2 - Carrier Detect On-Off Delay - 20 MS
T3 - Poll Request Message Period - 70 MS
T4 - Poll Request Transmission Period - 115 MS
T5 - Poll Response Message Period - 150 MS
T6 - Poll Response Transmission Period - 495 MS
T7 - Poll Session Period - 610 MS

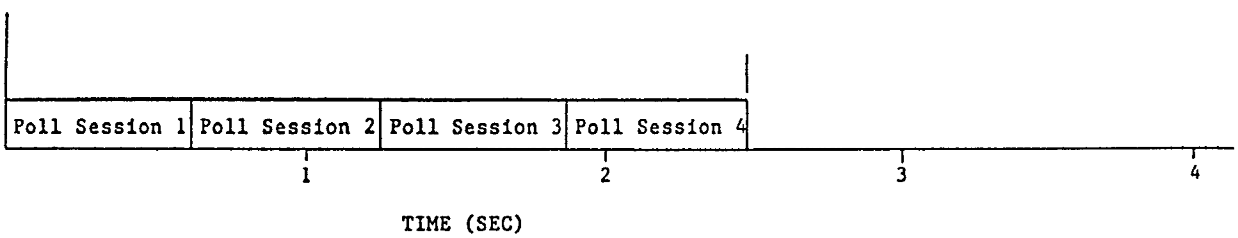


Figure 3-1. Poll Timing

A microprocessor in the CPU function (hereinafter referred to as processor) constantly monitors the energy used in heating the elements as well as the environmental parameters of temperature and pressure to compute the wind velocity. To ensure that the wind sensor meets the accuracy requirements, each sensor has been individually characterized and calibrated. The processor uses this information to ensure that the wind velocity it reports is within the specifications.

The element drivers contain the circuitry required to maintain the elements at the temperature specified by the processor. They also provide a measure of the amount of energy required to maintain the temperature. The input/output (I/O) busses allow the processor to specify the element temperatures, and the voltage across each element (V ELEMENT, shown in FIGURE 3-2) is a measure of the energy required to maintain the element temperature. The temperature circuit provides the means for the processor to determine the ambient temperature. The temperature circuit provides a voltage output proportional to ambient temperature (VT) as well as the temperature circuit reference voltage (VT REF).

The barometric pressure circuit provides a means for the processor to determine the ambient pressure. The barometric pressure circuit provides a voltage output (VBARO) proportional to barometric pressure. The PCP output to the control/status function is a status output.

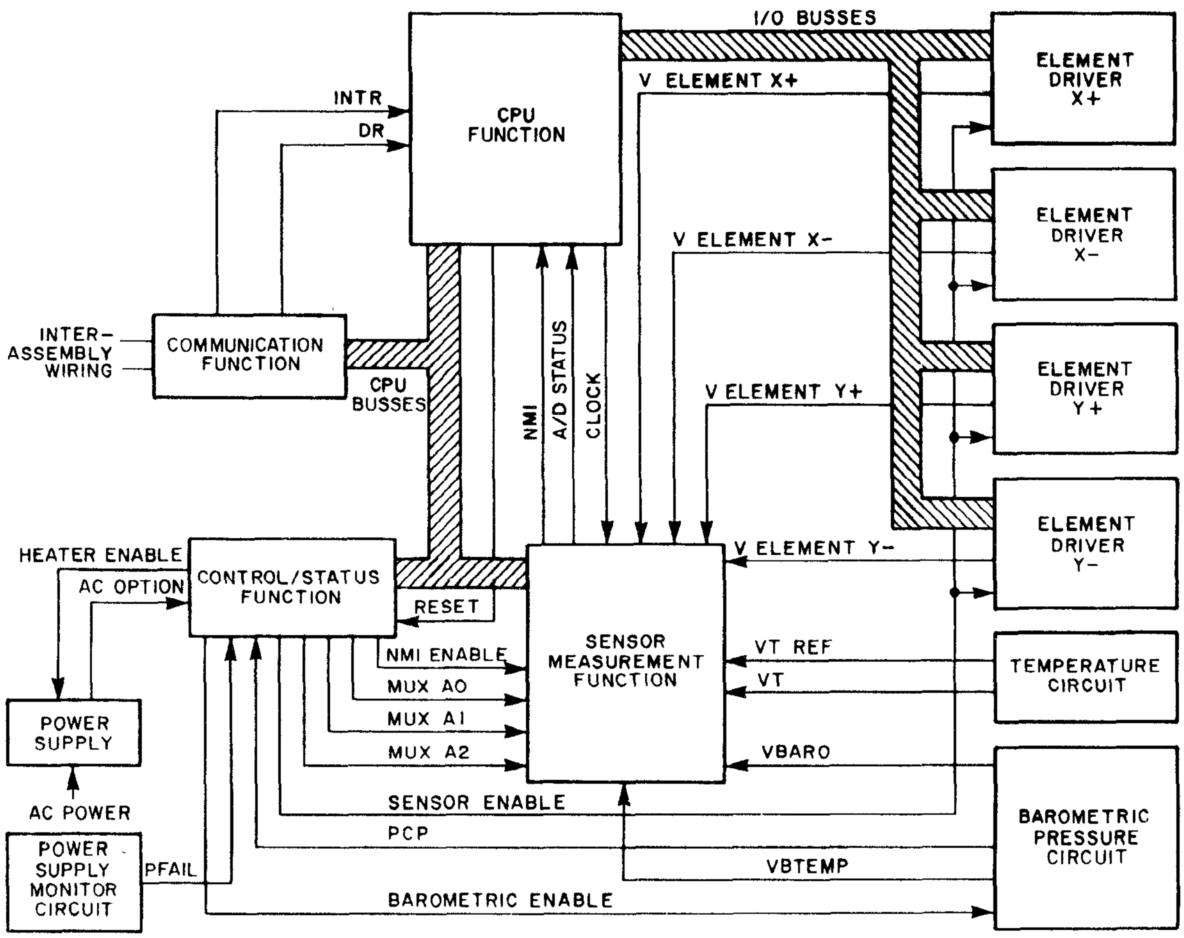


FIGURE 3-2. Sensor Overall Block Diagram

The measurement function converts the voltages and the frequency from the temperature and barometric pressure circuits, respectively, into digital words required for processing by the processor. The measurement function also provides system timing.

Selection of the voltage to be measured by the measurement function is determined by the control/status function. The control/status function also provides enable signals required by other sensor functions. The control/status function also allows the processor to determine the sensor's identification (I.D.). This allows the sensor to respond to polls which are addressed to it by either the master indicator or recorder. Communication between the sensor and the master over the inter-assembly data communications wiring is provided by the communications function.

The power supply provides the required DC voltages for the sensor's electronic circuits. These DC supplies operate from the AC power source.

The power supply failure circuit detects voltage levels that are outside nominal operating range and assert the signal PFAIL*.

3-2.2 **Sensor Element Drivers**. (See FIGURE 3-3.) FIGURE 3-3 is a block diagram of a typical element driver. Since the sensor includes four elements (X+, X-, Y+, and Y-), four element drivers are used.

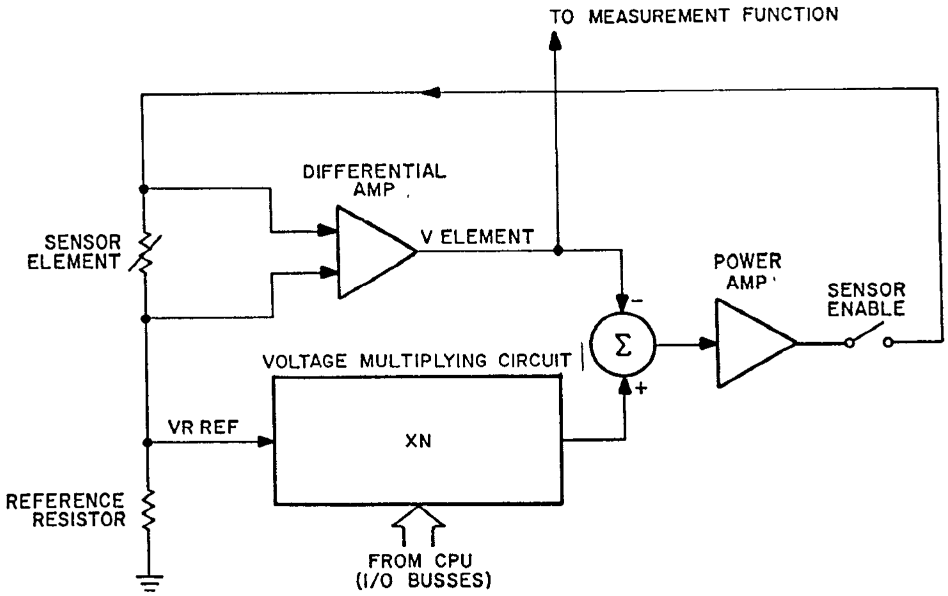


FIGURE 3-3. Sensor Element Drivers, Block Diagram

The heart of the element driver circuit is the sensor element pairs themselves. FIGURE 3-15 shows a detail of the sensor element pair construction. As shown, the sensor element consists of a ceramic tube covered with a platinum film coated with tempered glass. Two sensor elements are bonded together to make one of the two element pairs used in the sensor. Platinum is used since it is a stable metal with a significant temperature coefficient. The stability of the platinum is important to ensure the long-term stability of the wind sensor. The glass provides a protective coating for the platinum to prevent contamination from occurring.

Two elements are used together as a pair in order to sense the direction of the air flow. The windward element of the pair requires more energy to maintain its temperature above ambient (overheat) than the leeward element. The elements are joined in a fashion to prevent air flow between them. This ensures that the windward element of the pair has air flow over a greater surface area than the leeward element.

The circuitry used to drive the elements (FIGURE 3-3) maintains an element at a set temperature and senses the power required to maintain the set temperature. Since the element has a significant temperature coefficient to its resistance, the temperature of the element can be determined from its resistance. Therefore, in order to maintain a set temperature, only a set resistance needs to be maintained.

The power applied to the element is V^2/R , where V is the voltage across the element and R is the resistance of the element. Since platinum has a positive temperature coefficient, increasing the voltage across the element increases the power applied to it This increases its temperature and therefore its resistance.

To measure the element's resistance, a resistor of known value is placed in series with the element. By knowing the voltage across the reference resistor (VR REF), its resistance (R), and the voltage across the element (V ELEMENT), the element's resistance (RE) can be determined by the equation:

$$RE = \frac{\text{V ELEMENT}}{\text{(VR REF)/R}}$$

The power amplifier in the circuit ensures that V ELEMENT = N (VR REF), where N is a value determined by the processor. The processor not only has to know the element's temperature, it also has to be able to accurately set temperature in fine steps. The voltage multiplying circuit allows the temperature of the element to be set to within 0.1 degree C.

Since V ELEMENT = N (VR REF), RE = N (R). Likewise since R is known and N is set by the processor, RE is known. If V ELEMENT is measured, the power applied to the element is (V ELEMENT) ^{2}/RE. This power (the power required to maintain the element at the elevated temperature) is a measure of wind speed. The sensor enable switch is turned off whenever the microprocessor is reset. This is a failsafe protection feature to ensure that a valid value for N is always used.

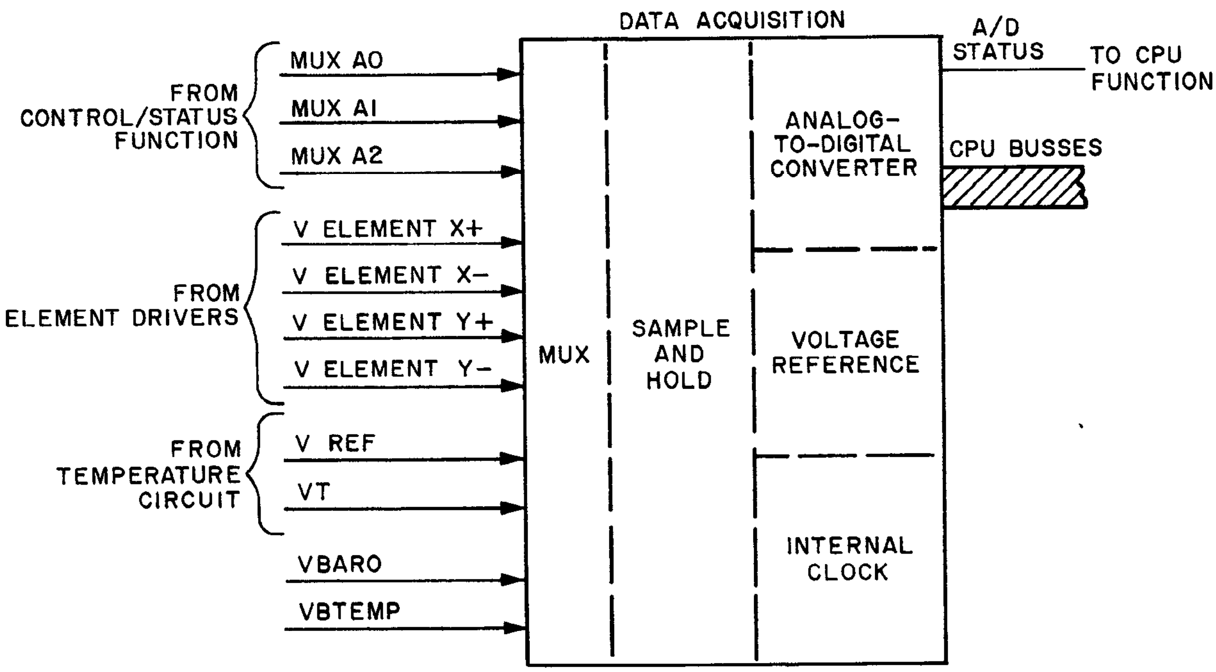
3-2.3 **Measurement Function**. (See FIGURE 3-4.) The measurement function provides the ability to measure voltage, frequency, and time. The data acquisition system (DAS) consists of a multiplexer, a sample and hold circuit, an internal clock, a voltage reference, and the analog-to-digital (A/D) converter. The DAS measures the voltage from the element driver circuits, the temperature circuit, and from the barometric pressure sensor. The A/D status allows the processor to know when the A/D has completed its conversion.

The programmable interval timer provides timing interrupts through the non-maskable interrupt (NMI) to the processor. The NMI Enable switch ensures that the processor receives no timing interrupts after a reset until it has configured its interrupt vectors. This is required since the state of the timing circuit is undefined on power up.

3-2.4 **Temperature Circuit**. (See FIGURE 3-5.) The temperature circuit measures the temperature to a resolution of 0.04 degrees C. The temperature sensor (located on anemometer assembly) is a positive temperature coefficient resistor. The temperature sensor driver biases the temperature sensor with a low-level signal in order not to cause self-heating. It provides a VT REF output to indicate the drive level. The temperature conditioning circuit amplifies the output to a level appropriate for the measurement function.

3-2.5 **Barometric Pressure Circuit**. (See FIGURE 3-6.) The barometric pressure sensor is a strain gage transducer.

The precision voltage reference from the temperature circuit (VREF) is scaled and inverted by the voltage source of the barometric pressure circuit. This reference voltage establishes the amount of current used to bias the strain gage bridge which forms the pressure sensor. The reference voltage is also used by the differential amplifier to bias the output of the amplifier to increase the usable dynamic range of the pressure sensor. The output VBARO from the amplifier is proportional to pressure and the output VBTEMP from the current source is proportional to temperature of the pressure sensor. These two signals are fed to the measurement function circuit.



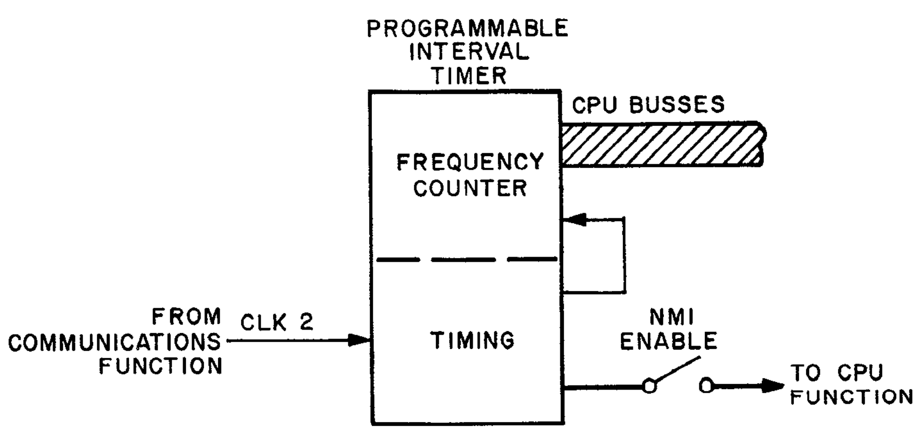


FIGURE 3-4. Sensor Measurement Function, Block Diagram

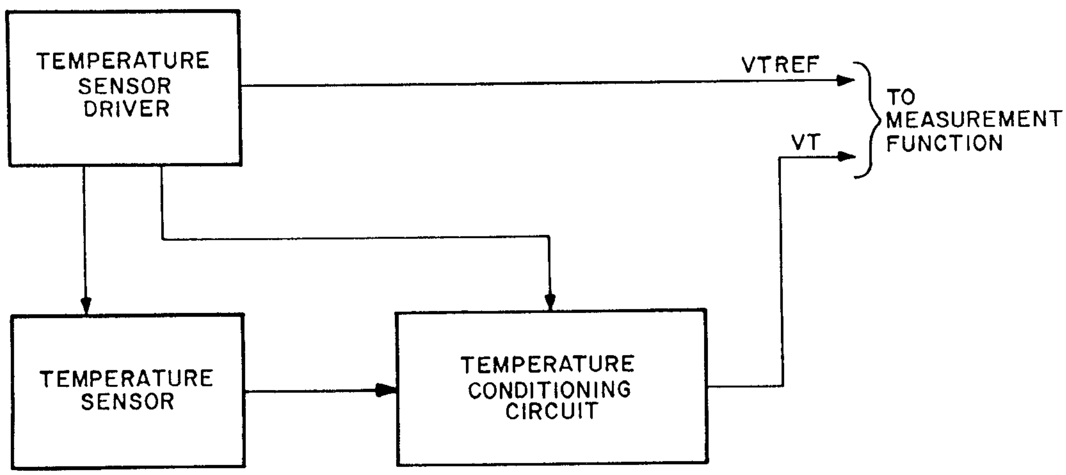


FIGURE 3-5. Sensor Temperature Circuit, Block Diagram

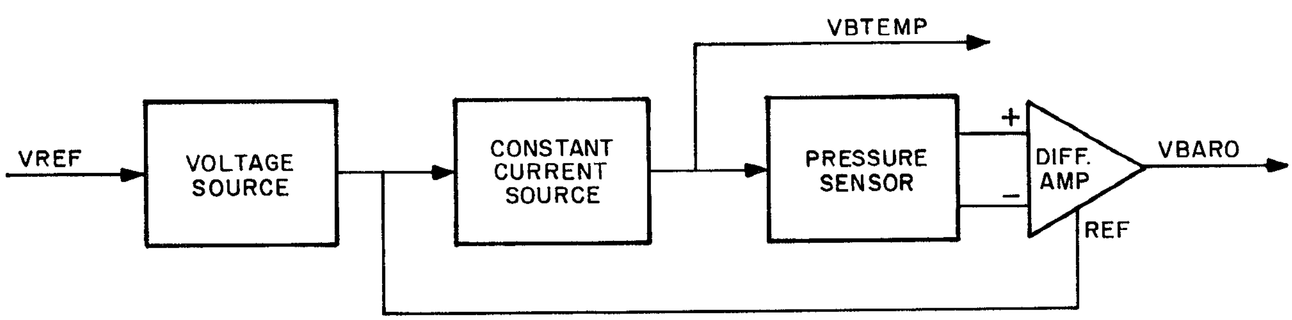


FIGURE 3-6. Sensor Barometric Pressure Circuit, Block Diagram

3-2.6 **Sensor Control/Status Function**. (See FIGURE 3-7.) The Sensor Control/Status Function consists of a status register and a control register. The status register provides status information to the processor via the multiplexed address/data bus, which includes status of the barometric pressure sensor and sensor identification. It also indicates whether the sensor is operating from 115 VAC or 230 VAC and reads test bits which are used for a self-test. The control register is used by the processor to set the mux address, enable the sensor, enable the barometric pressure circuit, enable the heater, and enable the timing interrupts. The control register is reset upon power-up and anytime the watchdog timer resets the processor. This ensures that the heater and the sensor elements are disabled unless the processor is functioning properly.

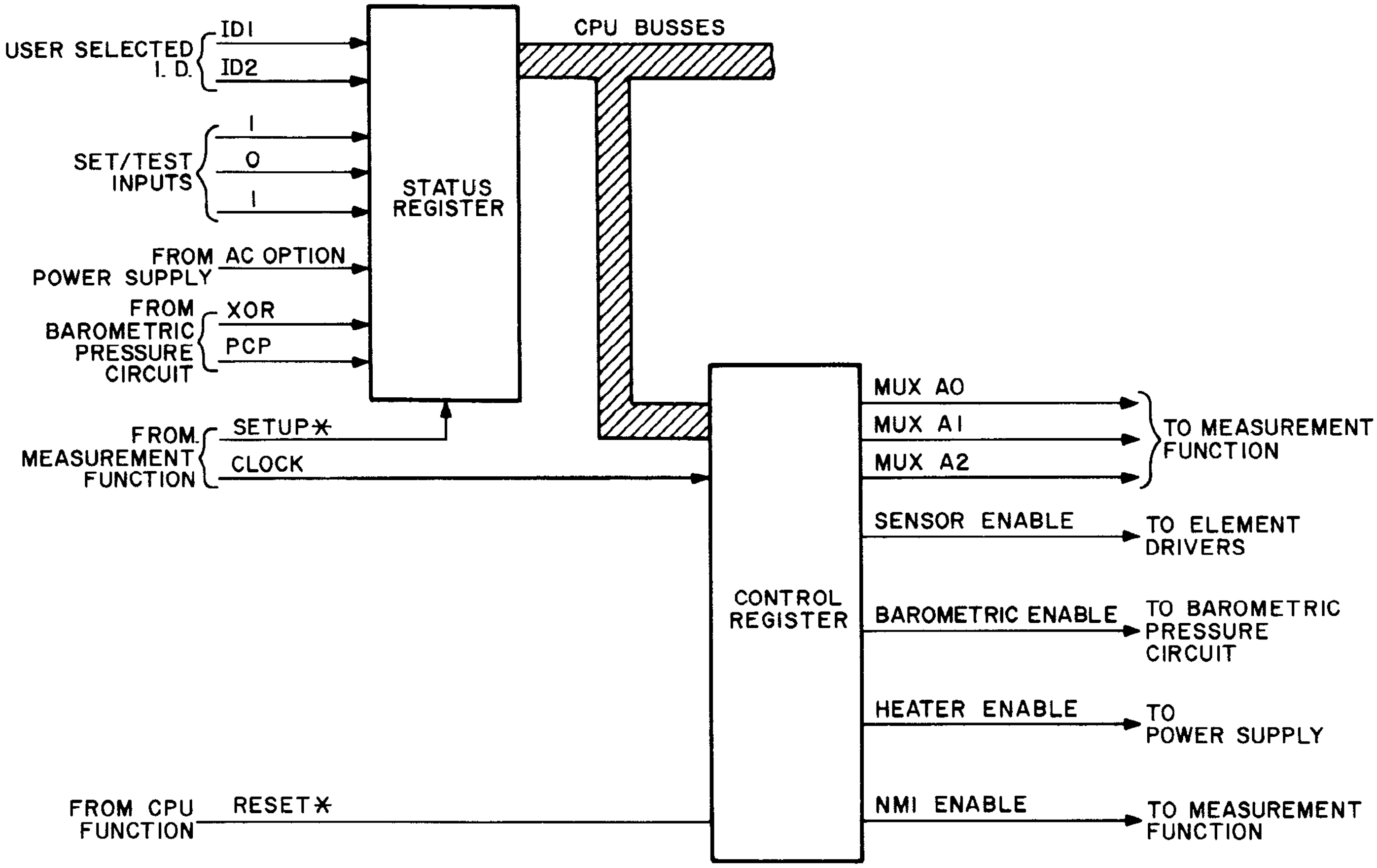


FIGURE 3-7. Sensor Control/Status Function, Block Diagram

3-2.7 **CPU Function**. (See FIGURE 3-8.) The CPU function is comprised of a microprocessor, clock generator, watchdog timer, memory chip select, I/O chip select, EPROM, RAM, I/O address and data bus buffer, and interrupt controller.

The heart of the CPU function is an 8/16 bit 80C88 microprocessor (hereinafter referred to as the processor). The processor includes a time-multiplexed data/address bus, an address bus, and a control bus. The processor executes its program from an Erasable Programmable Read Only Memory (EPROM). In addition to being the program memory for the processor, the EPROM contains the temperature vs resistance data of the elements, the temperature vs voltage data of the temperature circuit, voltage vs barometric pressure relationship of the barometric pressure, gains and offsets for D/A and A/D converters used in the element driver and measurement function, respectively, and calibration data for the sensor. The Random Access Memory (RAM) is the scratchpad memory for the processor. It is used to store data from the elements and for intermediate and final results of the calculations of wind speed and wind direction. EPROM and RAM memories are enabled by chip selects generated by the memory chip select circuit in response to inputs from the processor. The memory chip select circuit also provides chip selects for use in the inter-assembly communications function and for the A/D converter in the measurement function. The I/O chip select circuit provides chip selects for the D/A converters in the element driver function and for the watchdog timer.

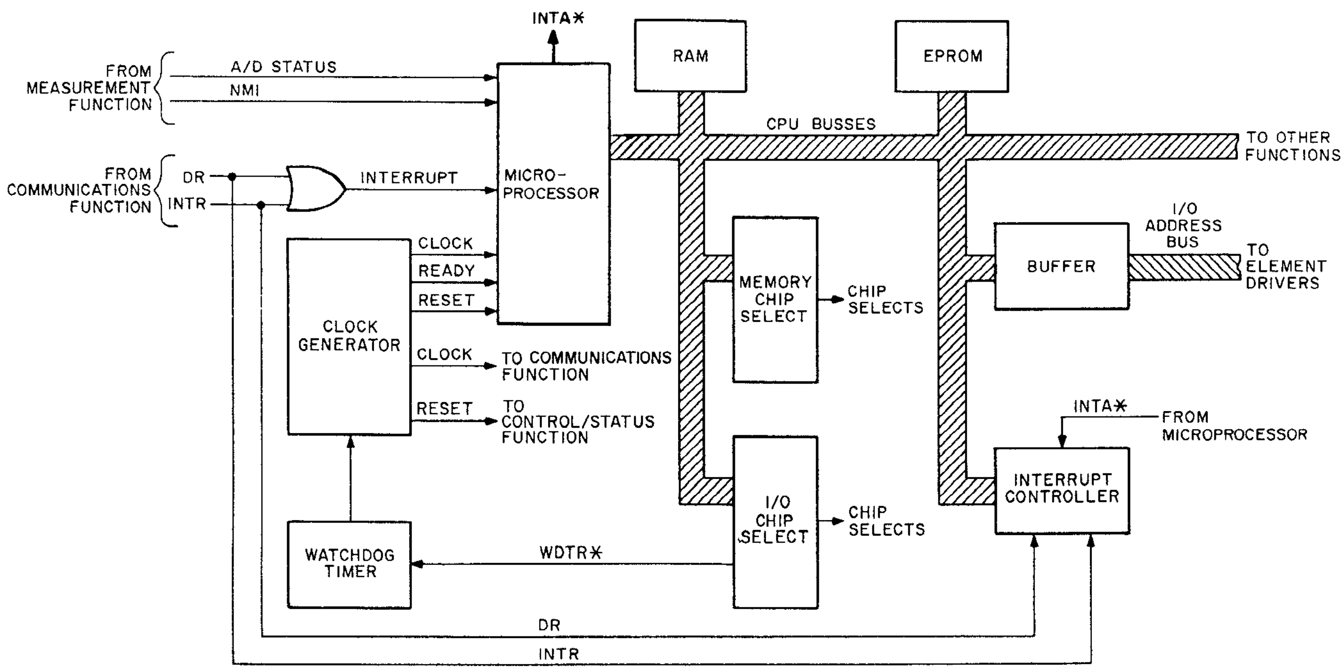


FIGURE 3-8. Sensor CPU Function, Block Diagram

All operations performed by the CPU are timed by a 4.9152 MHz clock generated by the clock generator. The clock generator is automatically reset by the watchdog timer if the processor is not executing proper software code. The clock generator routes Reset to the processor, and also provides Clock and Reset signals to other functions.

The processor has the built-in capacity to handle Interrupt Requests which are assigned by a level of priority. The Universal Asynchronous Receiver Transmitter (UART) in the inter-assembly communications function can interrupt the processor by asserting either Data Received (DR) or Interrupt Request (INTR). The processor acknowledges the Interrupt Request by returning an Interrupt Acknowledge (INTA) to the interrupt controller. The interrupt controller sends a number, depending upon the state of the DR and INTR inputs from the UART, to the processor via the multiplexed address/data bus. The processor software looks up the vector number in a lookup table and executes the appropriate action.

3-2.8 **Inter-Assembly Communications Function**. (See FIGURE 3-9.) The inter-assembly communications function is comprised of a serial interface (UART), modem, and a line termination circuit.

Each sensor measures both wind direction (0 to 360 degrees) and wind speed (0 to 99 knots) ~~or 0 to 150 knots)~~. Samples taken over a 5-second period are grouped and vectorially averaged. These 5-second averaged values are sent over the CPU bus to be converted into serial form by the UART and fed via the Transmit Data line to the modem.

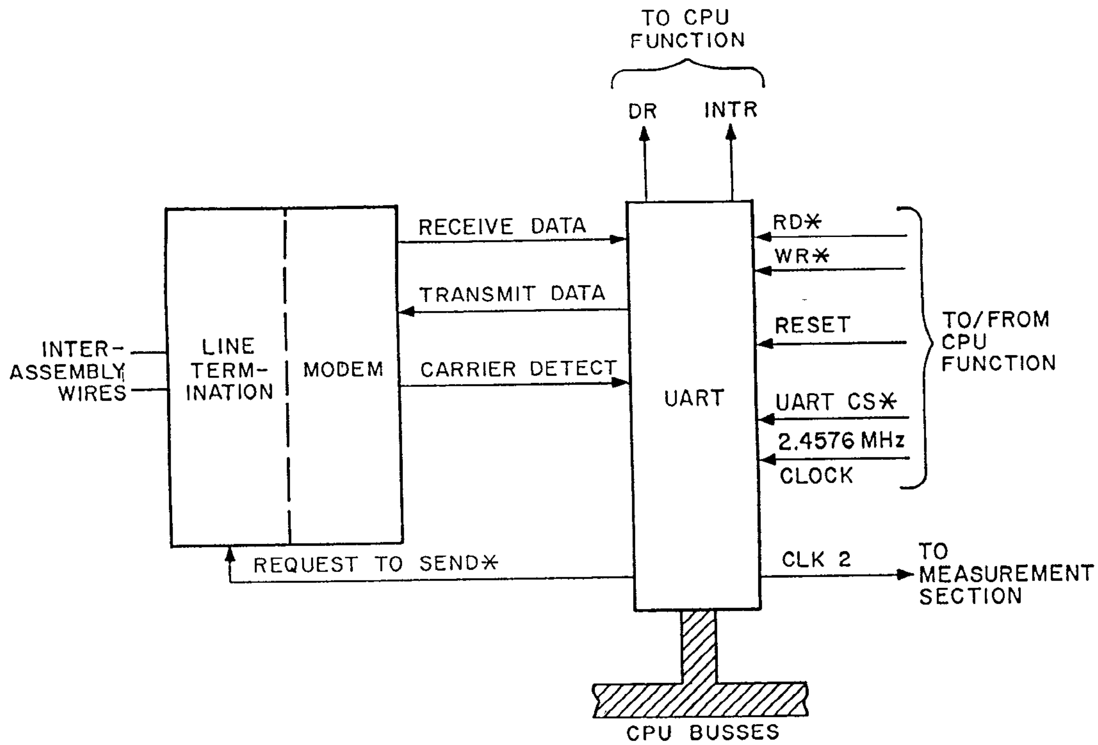


FIGURE 3-9. Sensor Inter-Assembly Communications Function, Block Diagram

The modem is a single chip Frequency-Shift Keying (FSK) voiceband modem which operates at 1200 bits per second (bps). The modem's transmitter is a programmable frequency synthesizer that provides one of two output frequencies, 1200 or 2200 Hz, representing the marks and spaces (which correspond to a logic "1" or logic "0," respectively) on the Transmit Data input. The receive section of the modem demodulates the analog signal, appearing at the Receive Data input, and is based on the principles of frequency-to-voltage conversion.

The FSK signal from the modem is fed to the inter-assembly data communications wires via a line termination circuit which provides the required gain adjustment and power drive capability.

When polled by the master indicator, the message received by the sensor is passed through the line termination circuit to the modem, which demodulates the received message and provides Receive Data to the UART, along with a Carrier Detect signal. The Carrier Detect signal is used to initiate transmission of an INTR signal from the UART to the CPU function. The UART receives Clock, Reset, Read (RD*), and Write (WR*) signals from the CPU function.

3-2.9 **Sensor Power Supply and Distribution**. (See FIGURE 3-10.) The sensor power supply operates from either 115 VAC or 230 VAC, 47-63 Hz, single phase and provides the following supply voltages:

a. +15 VDC at up to 100 milliamperes.
b. +12 VDC at up to 4 amperes.
c. +5 VDC at up to 350 milliamperes.
d. -15 VDC at up to 100 milliamperes.

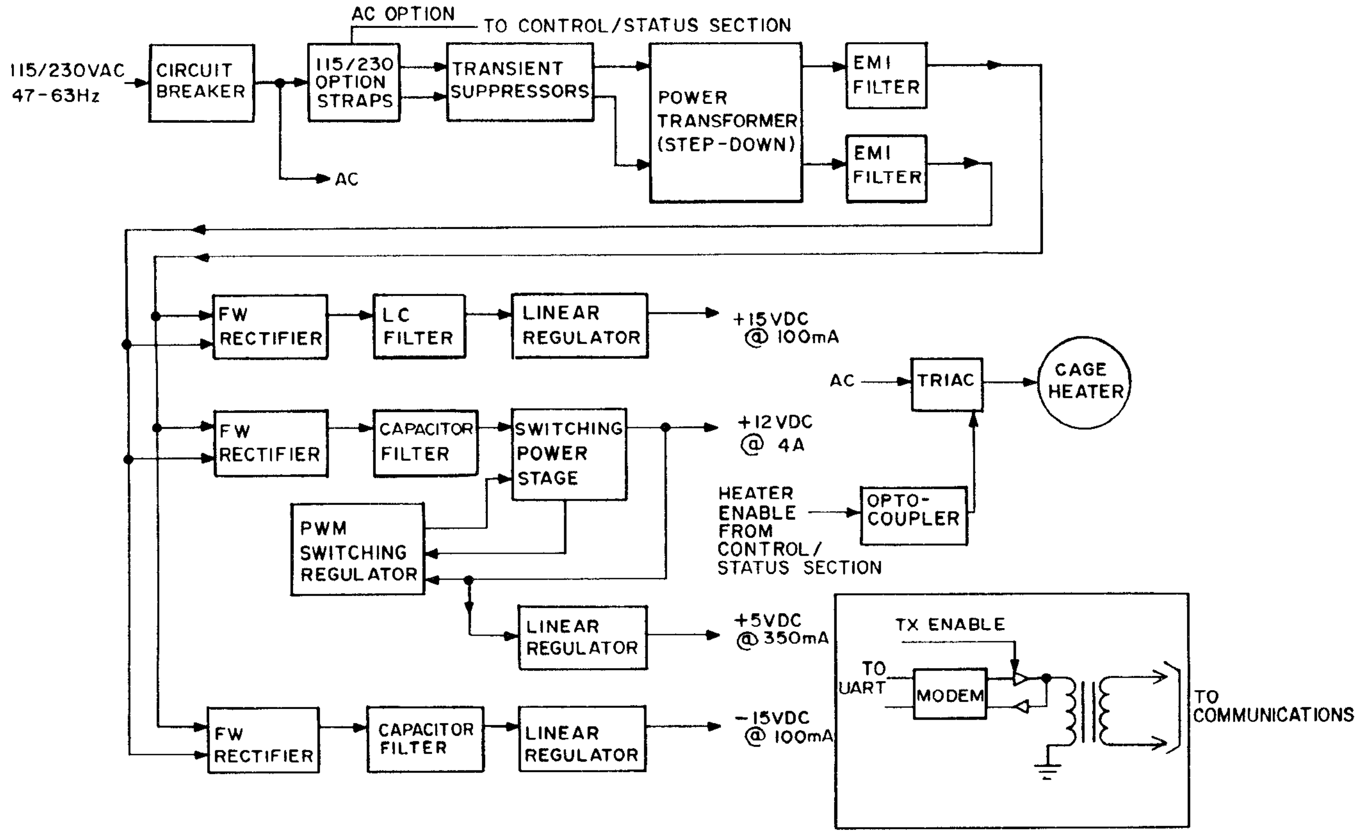


FIGURE 3-10. Sensor Power Supply and Distribution, Block Diagram

The AC input voltage is fed into the sensor through a circuit breaker. During installation, optional jumpers are connected for either 115V or 230V operation. The AC input is then fed via transient suppressors to the primary of a power transformer.

The stepped-down AC voltage developed across the secondary of the power transformer is fed to three full-wave rectifiers which provide rectification of the AC input voltage. The DC output of one full-wave rectifier is fed via an L-C filter to a linear regulator which provides +15 VDC at up to 100 milliamperes. Another linear regulator provides a -15 VDC, 100 milliampere output. This linear regulator receives a DC input from a full-wave rectifier via an L-C filter.

A switching regulator is used for the +12 VDC supply since it must supply high current (4 amperes). The +12 VDC output is also fed to the input of another linear regulator which provides +5 VDC at 250 milliamperes.

The power supply circuit also includes a triac which, when enabled, provides AC voltage to the cage heater.

3-3 <u>INDICATOR/RECORDER BLOCK DIAGRAM FUNCTIONING</u>.

Paragraph 3-3.1 provides an overall functional description of the indicator and recorder. This is followed by block diagram descriptions of the microprocessor PCBA, display PCBA, and power supply and distribution circuits, which are common to both indicator and recorder, with only minor differences.

3-3.1 **Indicator/Recorder Overall Block Diagram Functioning**. (See FIGURES 3-11 and 3-12.) The wind measuring set uses two versions of the indicator (dash 1 and dash 2). The dash 1 version is a standalone indicator. The dash 2 version is only slightly different from the dash 1 indicator and is used along with the printer to implement a recorder installation.

FIGURE 3-11 is a block diagram of the indicator. FIGURE 3-12 is a block diagram of the recorder. The printer is described in the printer commercial manual.

3-3.2 **Microprocessor PCBA Block Diagram**. Paragraphs 3-3.2.1 through 3-3.2.3 provide a block diagram of the indicator/recorder major functions.

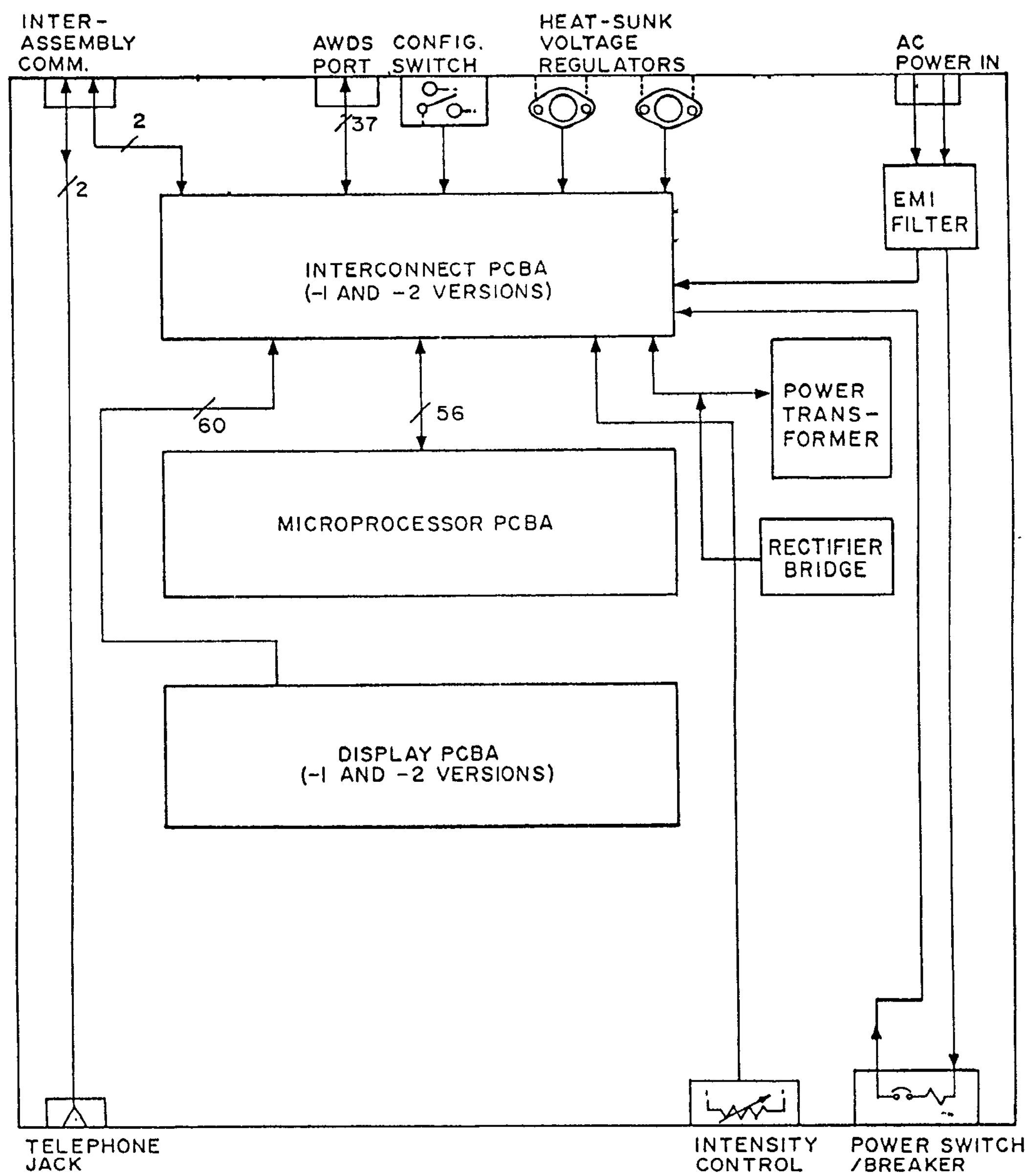


FIGURE 3-11. Indicator Overall Block Diagram

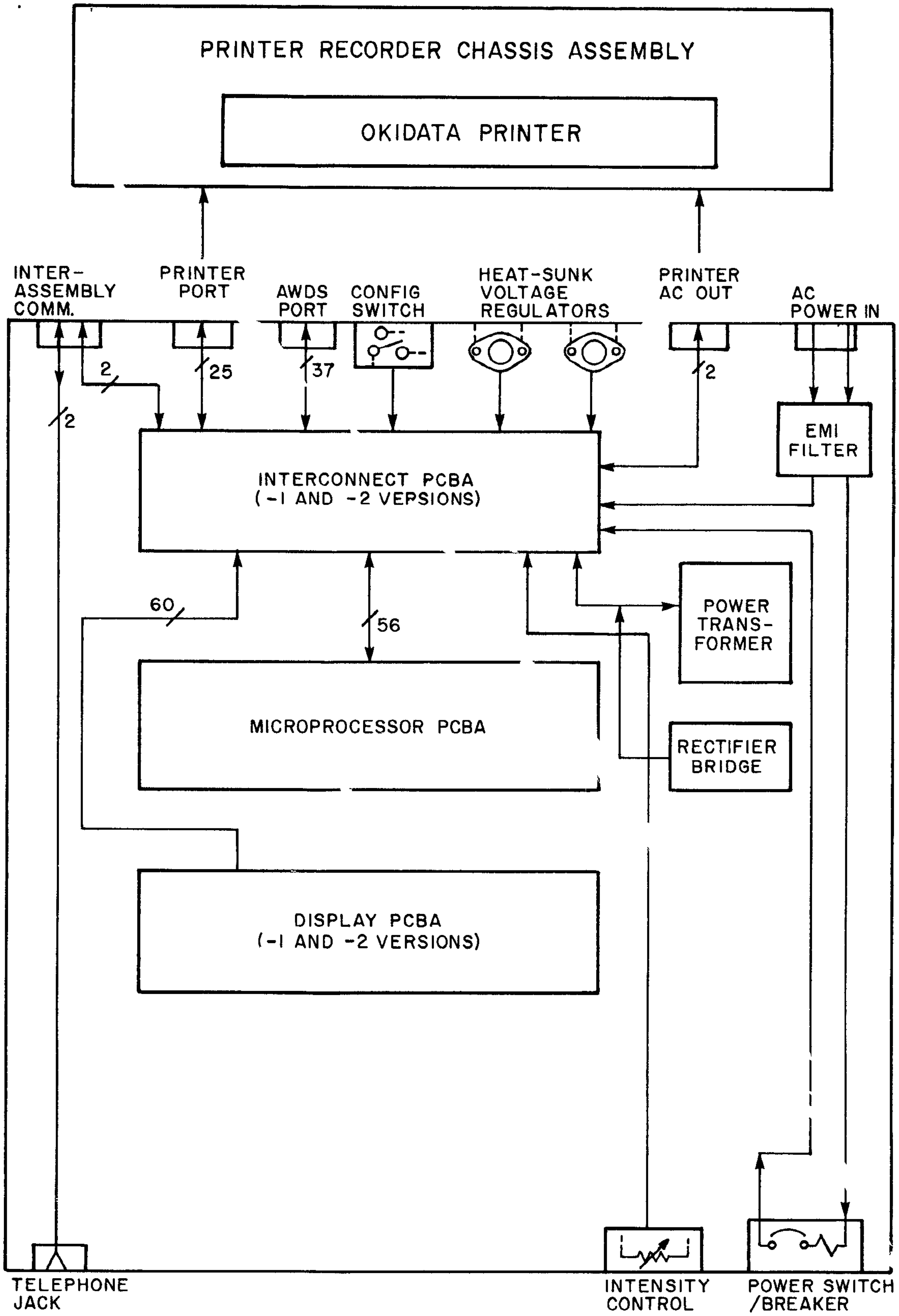


FIGURE 3-12. Recorder Overall Block Diagram

3-3.2.1 **CPU FUNCTION.** (See FIGURE FO-1) The CPU function is comprised of a microprocessor, address latch, watchdog timer and lockout circuit, clock generator, memory chip select decoder, RAM, EPROM, I/O chip select, real-time clock, battery backup circuit, and power supply circuits. The power supply circuits are described in paragraph 3-3.3.

The heart of the CPU function is an 8/16 bit microprocessor. The processor includes a time multiplexed data/address bus, address bus, and a control bus. The processor executes its program stored in an EPROM. The RAM is the scratch pad memory for the processor. The RAM stores weather data received from the active sensor and performs necessary calculations of peak wind and variability, etc. EPROM and RAM memories are enabled by chip selects generated by the memory chip select decoder in response to inputs from the processor. These chip select signals divide memory selection into two 32K byte segments, RAM being the lower order 32K of each page and EPROM being the high order 32K, for a total of 64K. The I/O chip select decoder generates chip select signals for each peripheral when the processor is addressing each of the individual peripherals on the I/O cycle.

The watchdog timer and lockout circuit automatically resets the microprocessor, multi-protocol serial controller (in I/O function), and display circuits after approximately 1/2 second if the CPU stops executing proper software for any reason. A 19.2 kHz clock from the modem circuit is counted by the watchdog timer. During normal operation, the I/O chip select decoder, under control of the processor, periodically outputs a Watchdog Timer Reset (WDTR*) signal which resets the watchdog timer, and the timer will never time out. If the software is not executing properly, the WDTR* signal is not generated and the RESET* pulse generated at the output of the watchdog timer is fed to the I/O function and display circuits. The RESET* pulse is also inverted to provide a logic "1" RESET pulse which resets the processor.

The lockout circuit generates signals which initialize the processor and lock out the processor from the RAM and real-time clock whenever input power is low. When a power failure, brown-out, or power-down occurs, the lockout circuit detects the condition before the +5V supply voltage to the digital logic drops below 4.75V and deselects both the real-time clock and RAM, preventing their contents from being changed. When power returns to normal operating levels, the processor is released from reset and this starts executing software at its reset initialization. A potentiometer sets the threshold level that the input voltage must drop to before the RAM and real time clock are disabled. During normal operation, LKOUT* will be high and LKOUT will be low.

All operations performed by the CPU are timed by a 4.9152 MHz clock generated by the clock generator. The clock generator also provides a 2.4576 MHz peripheral clock to the I/O function, inter-assembly communication function, and the display circuits. The 2.4576 MHz clock is also counted down in the clock generator to provide clock pulses of 2400 Hz and 19.2 kHz. The 2400 Hz clock is fed to the display circuits. The 19.2 kHz clock is fed to the watchdog timer and the inter-assembly communication function.

The processor has the built-in capacity to handle interrupt Requests, which are assigned a level of priority by the multi-protocol controller in the I/O function. Timed interrupts for the processor are controlled by the real-time clock. The real-time clock interrupt (RTCI*) is generated every 100 milliseconds and at other times when software is looking for a regular interval. This interrupt maintains important timing relationships in software.

During a power-down or power interruption, a long-life 2.7V lithium battery powers the RAM and real-time clock until AC power is restored.

3-3.2.2 **I/O Function**. (See FIGURE FO-1.) The I/O (input-output) function is comprised of a multi-protocol serial controller (MPSC) and MIL-STD-188-114 (RS-223) line drivers and receivers. The multi-protocol controller performs the following functions:

a. Converts parallel data from the multiplexed data/address bus (AD0-AD7) into serial asynchronous serial bit streams for transmission to the modem in the inter-assembly communications function and converts serial bit streams from the modem into parallel form for processing by the processor.

b. Converts parallel data from the multiplexed data/address bus (AD0 -AD7) into serial asynchronous serial bit streams for transmission to the AWDS port, and converts asynchronous serial bit streams from the AWDS port into parallel form for processing by the processor.

c. Adds the necessary start and stop bits to each character to be transmitted, and strips off those bits from the received characters.

d. Generates interrupt signals.

3-3.2.3 **Inter-Assembly Communications Function**. (See FIGURE FO-1.) The inter-assembly communications function consists of a Bell 202-type modem and a line termination circuit.

The modem is a single-chip asynchronous FSK voiceband modem which operates at 1200 bps. The modem's transmitter is a programmable frequency synthesizer that provides one of two output frequencies, 1200 or 2200 Hz, representing the marks and spaces (corresponding to a logic "1" and logic "0," respectively) on the modem's transmit data (TXD) input from the MPSC.

The FSK signal from the modem is fed to the inter-assembly data communications wires via a line termination circuit which provides the required gain adjustment and power drive capability.

The microprocessor turns the modem's output on and off via the Request to Send (RTS*) signal from the MPSC. This allows time sharing of the channel so that all sensors and the master indicator can transmit in turn on the inter-assembly data communications channel.

The receive section of the modem demodulates the FSK signals appearing on its receive (RXA) input and feeds this information in digital form to the MPSC. Carrier Detect information to the MPSC initiates an interrupt when the received signal amplitude is above a preset level. The modem will successfully demodulate signals over a wide dynamic range, 2.2V to 40 millivolts peak-to-peak amplitude (0dBm to -35 dBm). The modem includes four adjustment potentiometers: Transmit Level, Receive Level, Carrier Detect Threshold, and Receive Bias Distortion.

3-3.3 **Display PCBA Block Diagram Description**. (See FIGURE 3-13.) The display PCBA consists of a display controller and keyboard scanner, binary code decimal (BCD)-to-7-segment decoders, 14 current sources, 7-segment LED displays, digit select, intensity control, printer port, and alarm.

The keyboard portion of the display controller interfaces all front panel pushbuttons used by the operator. The display portion provides a multiplexed drive for the 7-segment LEDs. The circuit includes a 16 x 8 display RAM which can be loaded or interrogated by the processor via the multiplexed data/address bus (AD0 - AD7).

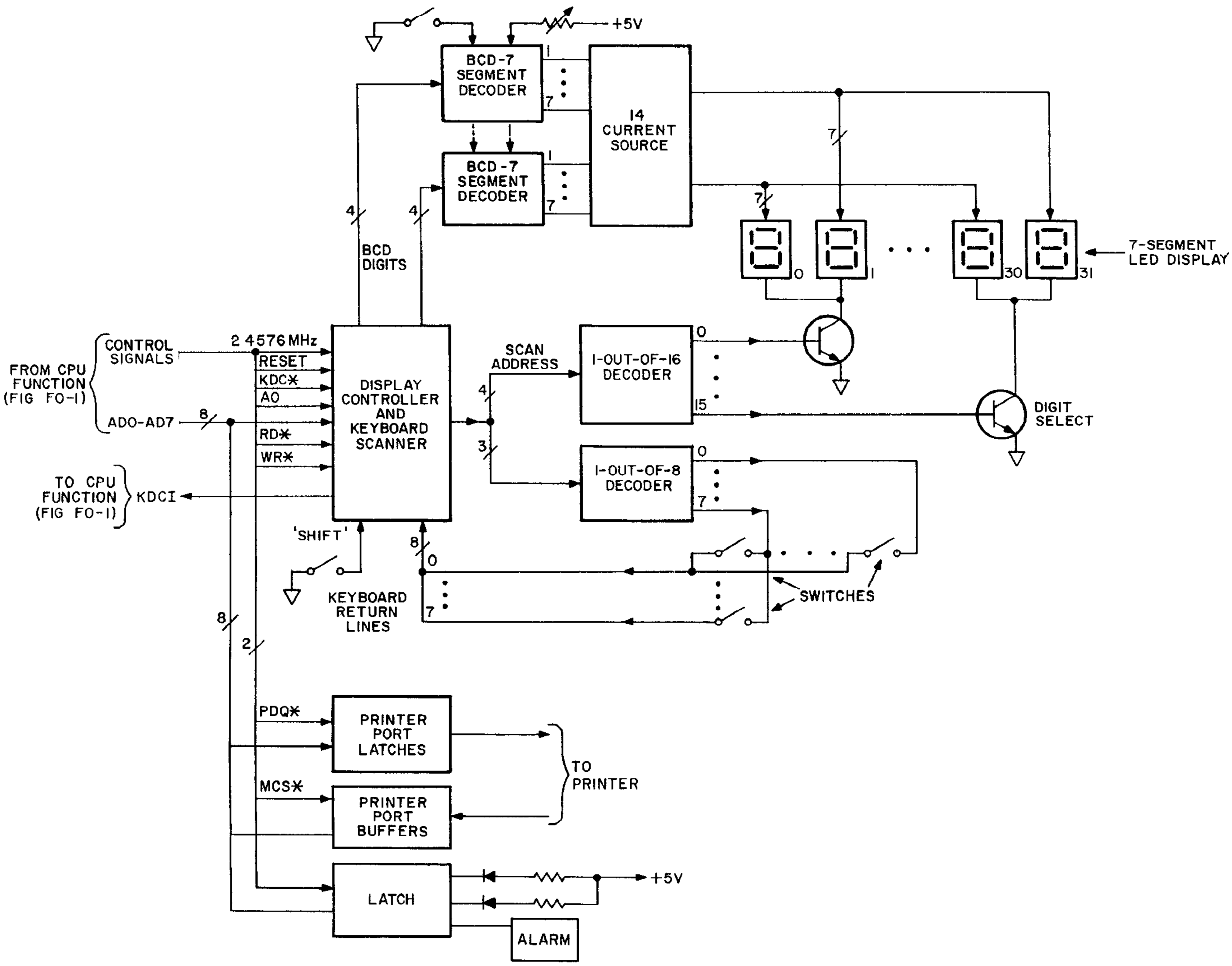


FIGURE 3-13. Indicator/Recorder - Display PCBA, Block Diagram

The BCD-to-7-segment decoders are used to decode the multiplexed BCD inputs from the display controller and keyboard scanner to a 7-segment output which determines which segments in the 7-segment display are turned on for each BCD input. The LAMP TEST pushbutton will turn on all segments of each 7-segment display when pressed, causing a number 8 to be displayed on each display.

There are 14 current sources, each turned on and off by a different output of the two 7-segment decoders. When turned on by the corresponding output of the BCD-to-7-segment decoder, the current source will provide approximately 200 milliamperes current drive for the 7-segment displays.

The 32 LED displays are arranged in two banks of 16 each. All the anodes of the LEDs in bank A are driven simultaneously and all anodes in bank B are driven simultaneously by the current sources. The cathodes of the LEDs are grounded through a transistor switch in the digit select circuit to allow current to flow through it. Only one cathode in each bank can be grounded at a time.

Thus, only one LED in each bank can be turned on at a time. The digit select circuit uses two 1-of-8 decoders to provide a 1-of-16 output corresponding to the BCD Scan Address from the display controller and keyboard scanner. The intensity of the 7-segment displays is controlled by duty cycle modulation. That is, by lengthening or shortening the duration of the pulse which turns on the LED, it is possible to control the time the LED display stays on, and thereby its intensity. The duration of this pulse is adjustable by the INTENSITY control.

The display PCBA in the recorder display unit includes a printer port to interface the AD0-AD7 bus with the printer connected to printer connector A3J3. The recorder display unit also includes an alarm circuit which provides a piezo-electric beeper under processor control.

All pushbuttons mounted on the front panel are continuously scanned by the keyboard scanner. When a pushbutton is pressed, the keyboard scanner initiates interruption of the processor.

3-3.4 **Power Supply and Distribution**. (See FIGURE 3-14.) The indicator/recorder power supply operates from either 115 VAC or 230 VAC, 47-63 Hz, single phase and provides the following outputs:

a. VLED (+5.25 VDC at up to 3 amperes).
b. D+5V (+5.0 VDC at up to .1 ampere).
c. A+5V (+5.0 VDC at up to 50 milliamperes).
d. +12V (+12.0 VDC at up to 50 milliamperes).
e. -12V (-12.0 VDC at up to 50 milliamperes).

The AC input voltage is fed into the indicator/recorder through an EMI filter and circuit breaker. During installation, optional jumpers are connected for either 115 VAC or 230 VAC operation. The AC input is then fed via transient suppressors to the primary of a power transformer. The stepped-down voltage developed across the secondary of the power transformer is fed to the input of the full-wave bridge rectifier which provides rectification of the input voltage.

The DC output of one full-wave rectifier is filtered by a filter capacitor and then fed to the input of three linear voltage regulators. The two chassis mounted regulators provide VLED (+5.25 VDC) and D+5V (+5.0 VDC). The regulator mounted on the microprocessor PCBA provides A+5V (+5.0 VDC). The DC output of the other full-wave bridge rectifier is similarly filtered and regulated to provide +12 VDC and -12 VDC.

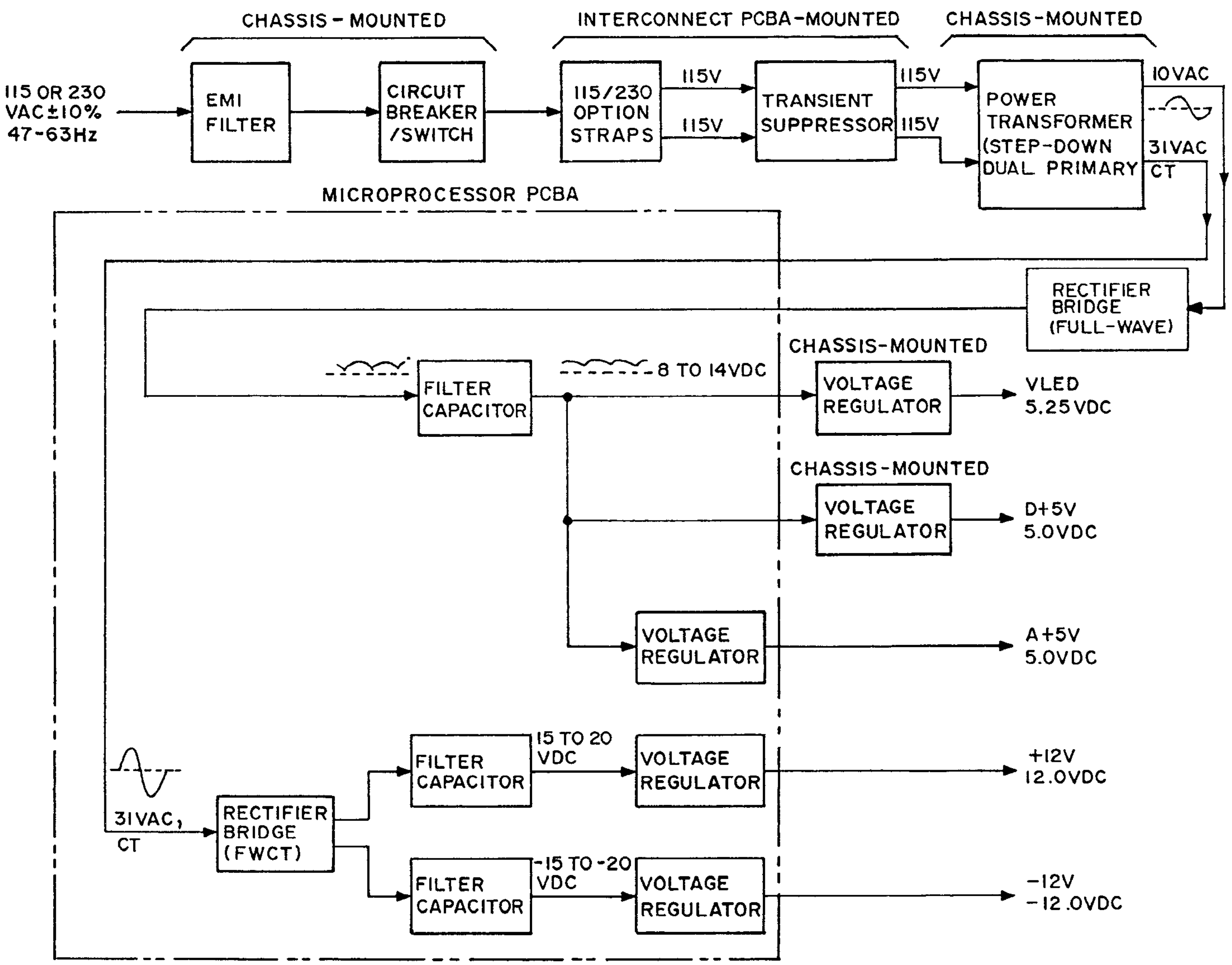


FIGURE 3-14. Indicator/Recorder - Power Supply and Distribution, Block Diagram

Section II. FUNCTIONAL OPERATION OF ELECTRONIC CIRCUITS

3-4 INTRODUCTION.

This section provides detailed functional descriptions for each unique PCBA used in the sensor, indicator, and recorder. Narrative descriptions are supported by signal flow diagrams and power distribution diagrams contained in the Circuit Diagrams Manual (T.O. 31M1-2FMQ13-3).

3-5 SYSTEM LOGIC LEVELS.

The wind measuring set uses the positive voltage level (+5 volts) as the logic "1" state (high level) and ground level as the logic "0" state (low level). Although the logic "0" state is said to be ground or zero volt, the level is usually within 0.4 volt of zero. If any signal is at the logic "1" state or high, the inverse or complement of the signal is "0" or low. The complement of any signal is indicated by means of an * placed after the signal name. For example, RESET* is logic "0" if RESET is "1," and vice versa.

3-6 SENSOR DETAILED FUNCTIONAL DESCRIPTION.

Paragraphs 3-6.1 through 3-6.9 describe the function of the sensor elements, sensor element driver function, sensor measurement function, temperature and barometric pressure circuits, control/status function, CPU function, communications function, and power supply/distribution function.

3-6.1 **Sensor Elements**. (See FIGURE 3-15.) As shown in FIGURE 3-15, the sensor element pair consists of a ceramic tube covered with a platinum film coated with glass. Two sensor elements are bounded together to make one of the two element pairs. Platinum is a stable metal with a significant temperature coefficient. The stability of the platinum is important to ensure the long-term stability of the wind sensor. The glass provides a protective coating for the platinum to prevent contamination from occurring.

Two elements are used together as a pair in order to sense the direction of the air flow. The windward element of the pair will require more energy to maintain its temperature above ambient (overheat) than the leeward element. The elements are joined in a fashion to prevent airflow between them. This ensures that the windward element of the pair has airflow over a greater surface area than the leeward element.

The two sensor pairs are used to sense the two orthogonal components of the wind. The X pair of elements is the East-West pair. The North edge of the X pair is designated X+; the South edge of the X pair is designated X-. The Y pair of elements is the North-South pair. The East edge of the Y pair is designated Y+; the West edge of the Y pair is designated Y-. Since there are two sensor pairs at right angles to each other, it is possible to calculate wind speed and direction.

3-6.2 **Element Driver Function**. (See FIGURE 3 of T.O. 31M1-2FMQ13-3.) The following paragraphs provide a detailed description of the sensor driver function. This detailed description is presented in the context of the overview and block diagram description given in paragraph 3-2.2. It is, therefore, recommended that paragraph 3-2.2 be reviewed before continuing with the following detailed discussion.

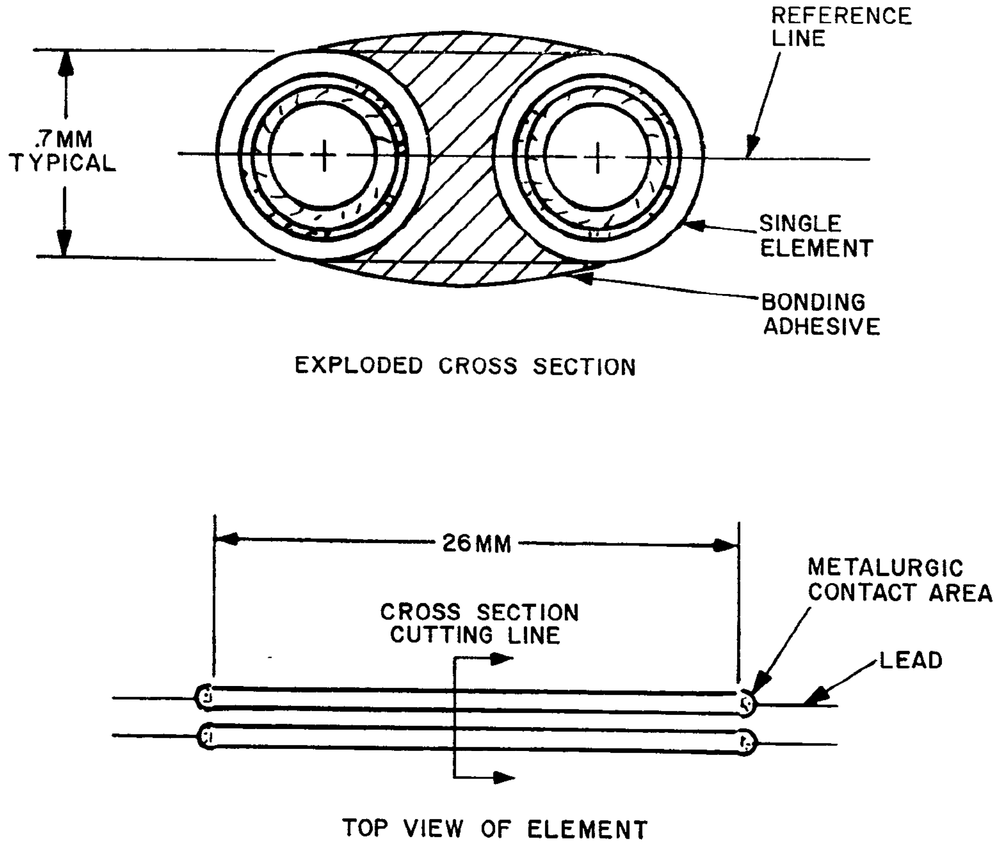


FIGURE 3-15. Detail of Element Construction

FIGURE 3 of T.O. 31M1-2FMQ13-3 is a detailed signal flow diagram of the element driver function. This diagram and the following descriptions cover only the X+ channel, which is typical of the four sensor element channels. For complete circuit details, refer to the microprocessor B PCBA schematic diagram in FIGURE 13 of T.O. 31M1-2FMQ13-3.

There are four connections to the X+ sensor element. A1-8 and A1-6 connect to one end of X+; A1-3 and A1-1 connect to the other end of X+. The differential amplifier connected across the sensor element is unity gain and non-inverting. It is comprised of U19-1, C47, and four 200K resistors in resistor network RN1. Capacitor C31 provides some high-frequency noise rejection. Resistor R5 and capacitor C25 comprise a low-pass filter for the signal being fed to the measurement function.

The reference resistor can be viewed as being comprised of R13, U15, and two 25K and two 200K resistors in RN1. U15 and the resistors of RN1 form a non-inverting amplifier with a gain of 8. This effectively increases R13 from 1 ohm to an 8 ohm reference resistor. U14 and U12-1 form the voltage multiplying circuit. U14 is a multiplying digital-to-analog converter (MDAC) with current outputs and internal feedback resistor. U12-1 converts the current to a voltage which, for this discussion, will be referred to as the output of the MDAC.

Being a 12-bit MDAC, values from 0 to 4095 can be loaded. The ideal transfer function is -VREF (N/4096), where N is the value loaded into the MDAC and VREF is the input voltage at pin 4 (output of U15). This particular MDAC is double-buffered, which means that it has digital input holding latches and an output latch. The processor writes the lower byte by selecting the MDAC (DAC0 CS* low) and by placing a high level on IOA (0). The processor then writes the high byte by selecting the MDAC and by placing a high level on IOA (1). The processor has now loaded the digital input latches and must assert (high level) LDAC in order to transfer the value from the digital input latches to the output latch. The summing at the input of the power amplifier is performed by the two 2K resistors in RN1. The power amplifier consists of U12-7, C24, R10, Q2, and Q1 (on power-back PCBA). U12 amplifies the error signal, while Q2 and Q1 provide the current drive capability.

Capacitor C24 provides some high-frequency filtering, while R10 improves the frequency response.

Capacitor C37 provides an integral action in the power amplifier, while R8 limits the gain of the power amplifier to the error signal. R3, R1, and Q1 implement the sensor enable switch. Resistor R3 provides the transition from logic levels provided by the control register to transistor levels. Q1 shorts the base of Q2, preventing power from being applied to the element, while R1 provides current limiting on the output of U12. R21 (on power-front PCBA) provides an initial biasing to bootstrap the circuit.

3-6.3 **Sensor Measurement Function**. (See FIGURE 4 of T.O. 31M1-2FMQ13-3.) As shown in FIGURE 4 of T.O. 31M1-2FMQ13-3, the sensor measurement function is comprised of a data acquisition circuit and a programmable interval timer. The data acquisition circuit is located on the microprocessor A PCBA. The programmable interval timer is located on the microprocessor B PCBA. These circuits are described in the following paragraphs.

3-6.3.1 **Data Acquisition Circuit**. The heart of the data acquisition circuit is an 8-channel, 12-bit data acquisition chip (U5) with interface logic to connect to the processor multiplexed data bus (AD0-AD7). It consists of an 8-channel multiplexer, a sample-and-hold amplifier, a 12-bit successive approximation analog-to-digital (A/D) converter, a voltage regulator, internal clock, along with the control logic needed to perform a complete data acquisition function.

The inputs to the 8-channel multiplexer of U5 are as indicated in table 3-3.

Table 3-3. Data Acquisition Input Channel Assignments

CHANNEL	DESCRIPTION
1	VELEMENT X+
2	VELEMENT X-
3	VELEMENT Y+
4	VELEMENT Y-
5	Temperature (VT)
6	Barometric Pressure Transducer Temperature (VTEMP)
7	Temperature Drive Reference (VT REF)
8	Barometric Pressure Voltage (VBARO)

Channels 1 through 4 of U5 receive a voltage related to the power required to maintain the sensor elements at a constant temperature. The X+ and X- inputs are for the North and South edge, respectively, of the East-West element pair. The Y+ and Y- inputs are for the East and West edge, respectively, of the North-South element pair. Channels 5 and 7 of U5 receive voltages corresponding to the drive level of the temperature circuit (VT REF) and actual ambient temperature (VT).

Channels 6 and 8 of U5 receive voltages from the barometric pressure circuit corresponding to the pressure (VBARO) and the temperature of the pressure transducer (VTEMP). The desired input voltage to be processed by the processor is selected by the MUX A0, MUX A1, and MUX A2 chip selects provided by the control/status function (paragraph 3-6.6) under control of the processor. A0 is part of the device address and also selects the conversion mode.

The logic level of the A0 line determines whether a 12-bit or 8-bit conversion will be initiated. If A0 is low during the start convert command, a 12-bit conversion will be started. If A0 is high, an 8-bit conversion will occur. The A0 line has to be set up when the R/C* line goes to logic "0" and must remain in the desired state for at least 150 nS. The R/C* line is used both to start a conversion and to read the output data. If R/C* is going low, a conversion is initiated. This is indicated to the processor by the A/D BUSY line going high. A second start convert command during a conversion will be ignored.

R/C*, in going high, initiates reading of multiplexed data from an internal register to an octal transparent latch with 3-state outputs (U1). When the OE* pin of U1 is driven low by a logic "0" chip select from U4B, the latched or transparent data is fed to the processor via the multiplexer bus (AD0-AD7). When OE* is high (logic "1"), the outputs of U1 are in the high impedance "off" state which means they will neither drive nor load the bus.

The chip select signals for U5 and U1 are provided by two 1-of-4 decoders in U4, with each decoder accepting two binary-weighted inputs (A0,A1) and providing two (actually four but two not used) outputs (Y0,Y1). Each decoder requires an active low on its CS* pin. In the case of decoder U4A, this is provided by a logic "0" WR* command from the processor in the CPU function (paragraph 3-6.7). In the case of decoder U4B, this is provided by a logic "0" A/D CS* from the memory chip select circuit in the CPU function. When A/D CS* is high (logic "1"), every output of U4 is high. The operation of the 1-of-4 decoders is shown in the following truth table.

INPUTS			OUTPUTS	
CS	A0	A1	Y0	Y1
L	L	L	L	H
L	H	L	H	L
L	X	H	H	H
H	X	X	H	H

The outputs of decoders U4A and U4B are used as follows (The A side consists of pins 1-7. The B side consists of pins 9-15.):

DECODER OUTPUT	DESCRIPTION
U4A, Y0	CLK to control/status function (U6)
U4B, Y0	OE* to U1
U4A, Y1	R/C* to U5
U4B, Y1	SETUP* to control/status function (U2)

3-6.3.2 **Programmable Interval Timer**. The programmable interval timer (U11) is used to provide timekeeping for the sensor, and also measures barometric pressure.

U11 uses three independent programmable and functional 16-bit counters to keep track of real-time from 1/4 second to 20 seconds. These counters are driven by the 19.2 kHz CLK2 clock from the UART in the inter-assembly communications function (paragraph 3-6.8) and are software programmable. Every 250 milliseconds and at other intervals set by software, U11 outputs an interrupt on its OUT0 pin which is ANDed in U18-6 with NMI Enable from the control/status function (paragraph 3-6.6) and used to interrupt the processor at regular preset intervals. Jumper J2 is set up for interrupts coming out of the counter. The CLK2 input is unused and is grounded through a 510K resistor.

The read/write logic of U11 accepts Read (RD*) and Write (WR*) inputs from the processor and generates control signals for other functional blocks of U11. A0 and A1 select one of the three interval counters or register to be read from/written into. A low on the RD* pin tells U11 that the processor is reading one of the counters or the status register. A low on the WR* pin tells U11 that the processor is writing either a control word or an initial count. Both RD* and WR* are qualified by CTR CS*. RD* and WR* are ignored unless U11 has been selected by holding CS low.

3-6.4 **Temperature Circuit**. (See FIGURE 5 of T.O. 31M1-2FMQ13-3.) The temperature circuit provides a reference voltage (VT REF) (corresponding to the temperature drive level) and a voltage (VT) which varies as the ambient temperature changes. The temperature circuit is located on the microprocessor A PCBA.

The ambient temperature is sensed by a thin-film resistance temperature-sensing element having a positive temperature coefficient of approximately 5000 parts per million.

The drive for the temperature sensor is provided from VT REF through R37, R29, C61, and C24 filter VT REF. R39, R41, and C32 are the passive components used to convert amplifier U12 into a gain and filter block. U12 is set up in an inverting amplifier configuration. R38 and R40 provide a positive bias to the non-inverting terminal to bias U12's output into the 0 to 10-volt range required by the measurement function. Capacitor C75 provides filtering of the voltage across the temperature sensor.

3-6.5 **Barometric Pressure Sensor**. (See FIGURE 5 of T.O. 31M1-2FMQ13-3.) This circuit allows the processor to compensate for changes in barometric pressure to prevent inaccuracies in wind data. The barometric pressure circuit is a separate PCBA module located on the microprocessor A PCBA. An overview of the operation of this circuit and a functional block diagram of the circuit is given in paragraph 3-2.5. The barometric circuit is comprised of the pressure transducer (U3), an instrumentation amplifier (U1), and two operational amplifiers (both contained in U2). The inputs to the pressure module are +15 volts, -15 volts, and analog ground. Digital ground and +5 volts are provided at the connector (E1-9 and E1-10), but are not used by the circuits on the module. The outputs from this circuit are VBARO and VBTEMP. The signal VBARO is proportional to the barometric pressure. The signal VBTEMP is proportional to the temperature of the pressure transducer. The response of the transducer is effected by its temperature. VBTEMP is used by the processor to compensate for this temperature sensitivity.

Reference voltage VREF is scaled and inverted by operational amplifier U2 (pins 1, 2, 3) to produce a reference voltage for the pressure circuit at the output (pin 1). This reference voltage is used by the operational amplifier U2 (pins 5, 6, 7) and R2 to form a constant-current source to bias the strain gage bridge of the pressure transducer. As the combined resistance of the transducer changes with temperature, the voltage at the output of U2 (pin 7) will change to maintain a constant current. This voltage is fed to the Data Acquisition Circuit as the signal VBTEMP. The output of U2, pin 1 is also applied to the reference input (REF) of instrumentation amplifier U1 to bias the output of the amplifier to be compatible with the 0 to 10-volt input range of the Data Acquisition Circuit described above in paragraph 3-6.3.1.

The pressure transducer is comprised of piezoresistive strain gages in the form of a Wheatstone bridge. Changes in the barometric pressure causes the voltage at the null points of the bridge to change. The output of the transducer is fed to the input of instrumentation amplifier U1. The voltage at the output of U1 is proportional to the barometric pressure. This output is connected to the Data Acquisition Circuit as the signal VBARO.

3-6.6 **Control/Status Function**. (See FIGURE 6 of T.O. 31M1-2FMQ13-3.) As shown in FIGURE 6 of T.O. 31M1-2FMQ13-3, the control/status function consists of a status register and a control register. These circuits are described in the following paragraphs. The control/status circuits are located in the microprocessor A PCBA.

3-6.6.1 **Status Register**. The status register uses an octal transparent latch with 3-state outputs (U2) to provide status information to the processor via the multiplexed data/address bus (AD0-AD7).

Jumpers J6 and J5 allow setting the sensor identification, IO1 and IO2, respectively. Jumper J4, J3, and J2 provide self-test inputs to the processor and is set up for a 1-0-1 code on the D3, D4, and D5 inputs of U2, respectively. The PCP input is a status input from the barometric pressure function (paragraph 3-6.5). PFAIL* is a status input from the power fail detector circuit of comparators in U18.

The active low SETUP* signal from the measurement function controls all eight 3-state buffers independent of the latch operation. When SETUP* is low, the transparent data appears at the outputs. When SETUP* is high, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

3-6.6.2 **Control Register**. The control register uses an octal D flip-flop (U6) to provide the following enable signals:

a. MUX A0, MUX A1, and MUX A2 Mux Address signals to the measurement function.

b. SENSOR ENABLE* to the element driver function.

c. NMI ENABLE to the sensor measurement function.

d. HEATER ENABLE to the power supply function.

e. Barometric Enable (B ENA) to the barometric pressure circuit.

The outputs of the control register are reset to zero whenever the processor is reset.

3-6.7 **CPU Function**. (See FIGURE 7 of T.O. 31M1-2FMQ13-3). As shown in FIGURE 7 of T.O 31M1-2FMQ13-3, the CPU function is comprised of a microprocessor, address latch, watchdog timer, clock generator, memory chip selector, Random Access Memory (RAM), Erasable Programmable Read Only Memory (EPROM), I/O chip select, and interrupt controller. The circuits comprising the

CPU function are located on the microprocessor B PCBA except for the watchdog timer which is located on the microprocessor A PCBA.

3-6.7.1 **Microprocessor**. The heart of the CPU function is an 80C88 CMOS 8/16 bit microprocessor (U2) (hereinafter referred to as the processor). The processor includes a time-multiplexed data/address bus (AD0-AD7), an address bus (A8-A15), and a control bus. The address generated by the processor is split between the highest 8-bit address byte (A8-A15) and the lowest 8-bit multi-plexed data/address bus (AD0-AD7). The processor executes its program from an EPROM, and stores its wind direction and speed calculations in external RAM. The data bus transfers data and status information. Memory and peripheral device addresses are transmitted via the address bus.

Accesses to memory are of two types: read and write. Access to external program memory (EPROM) uses a logic "0" Read (RD*) signal as the read strobe. Accessing the RAM uses Read (RD*) or Write (WR*) logic "0" signals to strobe the memory during read and write operation, respectively.

At the start of the processor cycle, the processor outputs an address on the multiplexed data/address bus. When the address is valid, the Address Latch Enable (ALE) output goes low, thereby latching the address into address latch U6. After ALE latches the address bus, the data bus portion (D0-D7) of the multiplexed bus (AD0-AD7) becomes enabled. Thus, in a write cycle, the data byte to be written appears on the AD0-AD7 bus just before the write strobe (WR*) is applied and remains there until after WR* is deactivated. As with the EPROM/RAM memories, an I/O (input-output) device is capable of placing data on the AD0-AD7 bus when a read (RD*) request is received. The IO/M* output of the processor is used to distinguish memory space from I/O space.

The processor receives two interrupt signals from the UART in the inter-assembly communications function: Data Ready (DR) and Interrupt (INTR). These two signals are ORed by diodes CR1 and CR2 to provide a logic "1" interrupt to the processor. The processor then acknowledges the interrupt by returning a logic "0" Interrupt Acknowledge (INTA*) to the interrupt controller. The interrupt controller sends a number (via the AD0-AD7 bus) to the processor. The processor software looks up the vector number in a lookup table and executes the appropriate action

The processor receives a logic "1" RESET input from the watchdog circuit via clock generator U3 if the software "crashes," or on starting up the unit after a power failure. The RESET input causes the processor to immediately initialize its present activity. All processor timing is controlled by a 4.9152 MHZ clock from the clock generator.

3-6.7.2 **Address Latch**. At the start of the processor cycle, the processor outputs a logic "1" ALE signal which allows latch U6 to accept the lower order address (A0-A7) appearing on the time-multiplexed data/address bus (AD0-AD7). ALE goes low (logic "0") to latch the lower order address byte. The address latch then holds the lower order address byte on the A0-A7 output bus until ALE goes high.

3-6.7.3 **Watchdog Circuit**. The watchdog circuit automatically resets the processor if there is a software problem If the software is operating normally, a WDTR* chip select signal is applied to the base of transistor Q7 through resistor R22, at least once every 200 milliseconds, which turns on the transistor. The resulting positive-going pulse at the collector of Q7 charges capacitor C19, which is then discharged through R7. The purpose of the R-C network comprised of C19 and R7 is to stretch the width of the pulse applied to the retrigger input of an astable multivibrator (U16).

As long as the retrigger input of U16 is pulsed, the Q output of U16 will be high. If, however, a software problem occurs, the WDTR* signal will not be generated and a logic "0" Reset (RES*) pulse is generated at the Q output of U16 which resets the clock generator (paragraph 3-6.7.4). On power up, the R-C time constant of R27 and C37 provides a power-up reset. Jumper J1 is the Watchdog Disable jumper. During normal operation, the jumper is removed. If it is ever desired to disable the watchdog timer during bench repair, a jumper is connected between pins 1 and 2 of J1. This keeps the retrigger input of U16 high, thereby preventing a logic "0" RES* signal from being generated at the Q output of U16.

3-6.7.4 **Clock Generator**. The clock generator uses a 14.7456 MHz crystal (Y1) to generate an internal 14.7456 MHz squarewave. The 14.7456 MHz squarewave is divided by three in a clock generator/driver (U3) to provide a 4.9152 MHz clock, whose frequency is just a little under the 5 MHz maximum signal of the 80C88 processor. This clock is an asymmetrical clock, high for one-third of the time and low for two-thirds of the time. The 14.7456 MHz is also divided by six in U3 to provide a 2.4576 MHz peripheral clock (PCLK) which is provided to the inter-assembly communications function (paragraph 3-6.8). The clock generator is reset when the RES* input from the watchdog circuit goes low. The clock generator also routes the RESET pulse to the processor. The RESET pulse at the R pin of U3 is also inverted by U10-2 to logic "0" and provided to the control/status function (paragraph 3-6.6).

3-6.7.5 **Memory Chip Select Decoder**. The 80C88 processor has the capability of addressing 1M of memory; however, only 8K RAM and 16K EPROM is addressed in this system. The memory chip select decoder uses a 1-of-8 decoder/demultiplexer (U5) to generate chip select signals for the RAM (RAM CS*) and EPROM. The EPROM chip select is generated by ANDing the Y6 and Y7 outputs of U5 in U18-3. The memory chip select decoder also generates chip select signals for the UART in the inter-assembly communications function (UART CS*), the programmable interval timer in the measurement function (CTR CS*), and the A/D (Analog-to-Digital) converter input in the measurement function (A/D CS*).

U5 has three enable inputs, two active low and one active high. Every output will be high unless the CS2* and CS3* pins are low and the CS1 pin is high. Since CS2* is permanently tied to ground, setting the IO/M* signal at CS3* low (logic "0") and the INTA* signal at CS1 high (logic "1") will enable U5. When enabled by a low IO/M* signal and a high INTA* signal from the processor, U5 will decode address bits A13, A14, and A15 to provide eight mutually exclusive active low outputs (Y0-Y7). The chip select signals generated are as follows:

U5 PIN	CHIP SELECT SIGNAL
Y0	RAM CS*
Y2	UART CS*
Y3	CTR CS* (Programmable Interval Timer)
Y4	A/D CS* (A/D converter)
Y6	CAL CS* (Calibration Data)
Y7	ROM CS* (Program Data)

The EPROM chip select is derived by ANDing the two most significant outputs (Y6 and Y7) of U5. This is necessary since either a 8K x 8 or 16K x 8 EPROM can be plugged into the EPROM socket.

3-6.7.6 **RAM**. The CPU function uses a type 6116 2K x 8 RAM chip (U1) as the scratchpad memory for the 80C88 processor. RAM address space starts at location 0 and stops at location 1FFF(H). The microprocessor PCBA can also be set up to use a type 6264 8K x 8 RAM; however, there is no defined use for the larger RAM at this time since all specified functions can be performed with the 2K x 8 chip. To accommodate the larger RAM, the jumper connected between pins 2 and 3 of jumper J1 must be unsoldered and connected between pins 1 and 2 of J1. The RAM stores whatever data is needed for communication or to perform the calculations of wind speed and wind direction.

RAM chip U1 is enabled by the RAM CS* chip select signal from the memory chip select decoder(paragraph 3-6.7.5). Address lines A0-A12 are used to select the location in the RAM that is to be accessed. Data are written into or read from memory depending on the WR* (Write) or RD* (Read) signals from the processor. These signals are logic "0" when active.

3-6.7.7 **EPROM** The CPU function can be configured with either a type 2764 8K x 8 or type 27128 16K x 8 EPROM chip (U17), but will be shipped with the 27128 chip installed. EPROM address space starts at C000(H) and stops at FFFF(H). The EPROM is the program memory for the 80C88 processor, and contains the temperature vs resistance data of the elements, the temperature vs voltage data of the temperature circuit, voltage vs barometric pressure relationship of the barometric pressure circuit, gains and offsets for the D/A and A/D converters, and the calibration data for the sensor.

There are two control signals provided to the EPROM, a chip select (provided by ANDing the two most-significant outputs of the memory chip select decoder in U18-3) and RD* (Read). Both control signals, being low (logic "0"), will allow program information or calibration information in the EPROM to be read back to the processor via the multiplexed data/address bus (AD0-AD7). Address lines A0-A14 are used to select the location in the EPROM that is to be accessed.

3-6.7.8 **I/O Chip Select**. A 1-of-8 decoder/demultiplexer (U4) is used to generate chip select signals for the digital-to-analog (D/A) converters in the sensor element driver function (paragraph 3-6.2) and for the watchdog circuit. U4 has three enable inputs, two active low and one active high. Every output will be active high unless the CS2* and CS3* pins are low and the CS1 pin is high. Setting the IO/M* signal at CS1 high, the ALE signal at CS2* low, and the WR* signal at CS3* low enables U4. When enabled, U4 decodes address bits A4, A5, and A6 to provide six mutually exclusive active low outputs (Y0-Y5). The chip select signals generated are as follows:

U4 PIN	CHIP SELECT SIGNAL*
Y0	DACO CS* (D/A converter 0)
Y1	DAC1 CS* (D/A converter 1)
Y2	DAC2 CS* (D/A converter 2)
Y3	DAC3 CS* (D/A converter 3)
Y4	LDAC* (Load D/A converter)
Y5	WDTR* (Watchdog Timer)

The Y4 output of U4 is fed via inverter U10-4 to provide a logic "1" LDAC signal to the sensor element driver function.

3-6.7.9 **Interrupt Controller**. The interrupt controller uses an 8-bit latch (U7) with 3-state outputs to send a vector number to the processor depending on the two interrupt signals, DR and INTR from the UART in the inter-assembly communications function (paragraph 3-6.8). The DR and INTR signals are fed to the two least significant latches of U7. The D6 pin is connected to +5V and the other D pins are tied to ground. This biases up the addresses to 32 and above.

Data on the D inputs are transferred to the latch outputs when INTA* from the processor is high. The latch remains transparent to the data inputs and the outputs are disabled while INTA* is high.

When the processor senses an interrupt, it causes INTA* to go low and the latched vector number of the interrupt is fed to the processor via the multiplexed AD0-AD7 bus. Since the first 32 vectors (0 through 31) are biased up, the DR and INTR interrupt inputs produce vectors numbers 33 and 34, or 35 if they both occur at the same time.

3-6.8 **Inter-Assembly Communications Function**. (See FIGURE 8 of T.O. 31M1-2FMQ13-3.) As shown in FIGURE 8 of T.O. 31M1-2FMQ13-3, the inter-assembly communications function is comprised of a serial controller interface, modem, and line termination circuit.

3-6.8.1 **Serial Controller Interface**. The serial controller is located on the microprocessor B PCBA. The modem and line termination circuits are located on the front power PCBA. The circuits comprising the inter-assembly communication function controller is a Universal Asynchronous Receiver Transmitter (UART) and Baud Rate Generator in a single chip.

The UART converts parallel data from the multiplexed data/address bus (AD0-AD7) into serial asynchronous serial bit streams for transmission to the modem and converts serial bit streams from the modem into parallel form, for processing by the processor.

Transfer of information between the UART and the processor is controlled by RD* and WR* commands provided by the processor. A RD* causes the UART to output data to the AD0-AD7 bus. A WR* command causes data on the AD0-AD7 bus to be input to the UART. U9 must be enabled by a logic "0" UART CS* from the CPU function to read or write data. The data input or output depends on the address inputs (A0, A1).

A low (logic "0") Carrier Detect signal (CDT) from the modem indicates that a data carrier signal has been detected and that a valid signal is present on its RXD line.

Receipt of a low CDT signal on the DSR* pin of U9 causes the INTR pin of U9 to go high. This is applied to the INTR pin of the processor. The DR pin of U9 goes high when a character has been received and is ready to be transferred to the CPU. Data from the modem comes in serially to U9 on the SDI pin. The UART strips off the start and stop bits and provides data from the modem to the processor in parallel form via the AD0-AD7 bus. Transmit data from the UART is fed serially to the modem via the TXD pin.

All operations performed by U9 are controlled by a 2.4576 MHz Peripheral Clock "PCLK" from the CPU function. This clock is also divided in U9 and fed via the CO pin to the programmable interval timer in the measurement function.

3-6.8.2 **Modem**. The inter-assembly communications function uses a single chip FSK voiceband modem (U3) which operates at 1200 bps. It uses silicon gate Complimentary Metal Oxide Semiconductor (CMOS) technology to implement a switched capacitor architecture. The modem's transmitter is a programmable frequency synthesizer that provides one of two output frequencies, 1200 or 2200 Hz, on TXA representing the marks and spaces (which correspond to a logic "1" or logic "0," respectively) on the TXD input.

The receive section of the modem demodulates the analog signal appearing at the RXA input and is based on the principle of frequency-to-voltage conversion. This section contains a group delay equalizer (to correct phase distortion), automatic gain control, carrier detect level adjustment, thereby optimizing performance and giving the lowest bit error rate.

The modem uses an external 4.4336 MHz crystal (Y1) frequency source. This crystal frequency drives an internal programmable frequency synthesizer that derives two output frequencies by variables of the 4.4336 MHz oscillator frequency. An on-chip oscillator runs from the external 4.4336 MHz crystal connected between the OSC1 and OSC2 pins to provide a 19.2 kHz clock from the CLK output which is 16 times the highest selected bit rate (transmit or receive). This 19.2 kHz clock is inverted via R19, Q6, and R17 and fed to the TRS pin to set the standard bit rates and mark-space frequencies.

3-6.8.3 **Line Termination Circuit**. The line termination circuit uses a pair of operational amplifiers (U2-7, U2-1) in a single chip that provide gain adjustment and power drive capability. The modem and line termination circuit are operated from a +5V supply and -12V supplies.

The TXA output of the modem is coupled through capacitor C9 and resistor R16 to operational amplifier U2-7. Potentiometer R8 is the Transmit Level adjust potentiometer. Potentiometer R8, in conjunction with resistor R16, sets the gain of operational amplifier U2-7 to O dBm output level (2.2 volts peak-to-peak).

Operational amplifiers U2-8 and U2-14 provide anti-streaming and level shifting functions in the control of Q7, under processor control, via the RTS* output of serial interface controller U9. When RTS* is set low by software, the gate of Q7 is pulled to +5V through 10K resistor R13, thus turning Q7 on and connecting the TXD (Transmit Data) output at U2-7 to transformer T1 which AC couples the transmit data to the inter-assembly data communications wiring. Transient suppressor CR2, connected across the transformer, provides transient suppression. It will take lightning pulses from the inter-assembly data communications wiring and short them out before they can damage the line transmission circuits.

If RTS* stays low for more than about a second, the R-C time constant of R7 and C8 is exceeded and the gate of Q7 is pulled to -15V, turning Q7 off and releasing the inter-assembly data communications channel so that another assembly may transmit. The R-C timeout protects the entire system from being disabled by a fault in a single assembly that keeps RTS* low and would otherwise allow the single faulty assembly to continuously "stream" its modem output onto the inter-assembly data communications wiring, thus disrupting any other assembly's transmission. When software completes a transmission, it normally sets RTS* back high, which immediately turns Q7 off and quickly discharges C8 through CR1 so that C8 is again ready to time the next RTS* pulse.

The Carrier On jumper (E10) is normally disconnected, but may be connected during depot repair or field installation to continuously enable the modem's output onto the inter-assembly data communications wiring for special test purposes. During depot repair, E10 can be connected to calibrate the inter-assembly circuit or to provide a test signal for troubleshooting. During installation, E10 can be connected to provide a constant test signal to check out the inter-assembly data communications wiring for opens, shorts, reflections, high loads, etc.

Data from the inter-assembly wiring comes into transformer T1, which AC couples the receive data to operational amplifier U2-1. The receive level is set by potentiometer R11 in combination with resistor R12. The output of U2-1 is fed into the RXA pin of the modem.

3-6.9 **Sensor Power Supply/Distribution**. (See FIGURE 9 of T.O. 31M1-2FMQ13-1.) The sensor power supplies operate from either 115 VAC or 230 VAC, 47-60 Hz, single phase.

The AC input voltage is fed into the sensor via the circuit breaker assembly. Input power is fed via E14 and E12 to the power front PCBA. During installation, optional jumpers (E15 and E25) are connected for either 115V or 230V operation.

The AC input to the power front PCBA is fed to a transient suppressor circuit comprising two varistors (RV1, RV2), two gas tubes (E11, E13), and two 7W wirewound resistors (R26, R27). The varistors have a fast response time but a low power dissipation. On the other hand, the gas tubes have a slow response time but have a high power dissipation. By using a combination of varistors and gas tubes, the transient suppressor circuit provides fast response to transients, while providing the required power dissipation.

When a transient appears on the AC input, varistors RV1 and RV2 turn on quickly to clamp the transients on the AC input to an acceptable level. Gas tubes E11 and E13 then turn on to dissipate most of the energy, and the varistors are relieved of this burden. Resistors R26 and R27 limit current through the gas tubes.

From the transient suppressor, the AC power is fed via J2 to two primaries in the transformer assembly. The transformer steps the AC input voltage down to a center-tapped AC voltage of approximately 36 VAC. The AC voltage from the step-down transformer is fed to the power back PCBA to three full-wave rectifiers which provide rectification of the AC input voltage.

The DC output of one full-wave rectifier is fed via a filter capacitor (C11) to linear regulator U5 (on the power front PCBA) which provides +15 VDC at up to 100 milliamperes. Another linear regulator (U6) on the power front PCBA provides a -15 VDC, 100 milliampere output. This linear regulator also receives a DC input from a full-wave rectifier via capacitor filter (C10).

A switching regulator (Q5) on the power back PCBA is used for the +12 VDC supply since it must supply high current (4 amperes). The +12 VDC output is also fed to the input of another linear regulator (U4) which provides +5 VDC at 350 milliamperes.

The power supply circuit also includes a triac (CR7) which, when enabled by Q5 and U1 on the power front PCBA, provides AC voltage for the cage heater. When the Enable Heater (EHT) signal from the control register in the control/status function is low, the heater is switched off. When EHT goes high, the heater is turned on to prevent ice from forming on the cage.

3-7 INDICATOR/RECORDER DETAILED FUNCTIONAL DESCRIPTION.

Paragraphs 3-7.1 and 3-7.2 describe the functioning of the microprocessor PCBA and display PCBA used in both the indicator and the recorder. Paragraph 3-7.3 describes the functioning of the indicator/recorder power supply and distribution circuits. Unless otherwise indicated, the descriptions apply to both indicator and recorder.

3-7.1 **Microprocessor PCBA**. The following paragraphs provide a detailed description of each of the major functions comprising the microprocessor PCBA used in the indicator and recorder.

3-7.1.1 **CPU Function**. (See FIGURE 19 of T.O. 31M1-2FMQ13-3.) As shown in FIGURE 19 of T.O. 31M1-2FMQ13-3, the CPU function is comprised of a microprocessor, address latch, watchdog timer, clock generator, memory chip select decoder, RAM, EPROM, I/O chip select decoder, real-time clock, and battery backup circuits. Each of these functions is described in detail in the following paragraphs.

3-7.1.1.1 **Microprocessor**. The heart of the CPU function is an 80C88 CMOS 8/16 bit microprocessor (U5) (hereinafter referred to as the processor). The processor includes a time-multiplexed data/address bus (AD0-AD7), an address bus (A8-A15), and a control bus. The address generated by the processor is split between the highest 8-bit address byte (A8-A15) and the lowest 8-bit multiplexed data/address bus (AD0-AD7). The processor executes its program from the 16K x 8 EPROM chips (U9), and makes its wind direction and speed calculations in the 8K x 8 RAM chip (U8). The data bus transfers data and status information. Memory and peripheral device addresses are transmitted via the address bus.

Accesses to memory are of two types: accesses to program memory (EPROM) and accesses to data memory (RAM). Accessing the EPROM uses a logic "0" RD* (Read) signal as the read strobe. Accessing the RAM uses RD* (Read) or WR* (Write) logic "0" signals to strobe the memory.
At the start of a processor bus cycle, the processor outputs an address on the multiplexed data/address bus. When the address is valid, the ALE (Address Latch Enable) output goes low, thereby latching the low byte of the address into address latch U7. After ALE latches the address bus, the data bus portion (D0-D7) of the multiplexed bus (AD0-AD7) becomes enabled. Thus, in a write cycle, the data byte to be written appears on the AD0-AD7 bus just before the write strobe (WR*) is applied and remains there until after WR* is deactivated. As with the EPROM/RAM memories, an I/O (input-output) device is capable of placing data in the AD0-AD7 bus when a RD* (Read) request is received. The IO/M* output of the processor is used to distinguish a memory from an I/O access.

The processor receives a logic "1" INTR (Interrupt) signal when an interrupt has been requested by the multi-protocol controller in the I/O function (paragraph 3-7.1.2). The processor then acknowledges the interrupt by returning a logic "0" INTA* (Interrupt Acknowledge) to the multi-protocol serial controller and requests the multi-protocol serial controller to indicate which interrupt occurred. The multi-protocol controller sends a vector number (via the AD0-AD7 bus) to the processor. The processor software looks up the vector number in a lookup table in RAM, reads the address of the corresponding routine, and calls up that routine. The processor receives a logic "1" RESET input from the watchdog circuit (paragraph 3-7.1.1.3) if the software "crashes" or on starting up the unit after a power failure. The RESET input causes the processor to immediately initialize its present activity. All processor timing is controlled by a 4.9152 Hz clock from the clock generator (paragraph 3-7.1.1.4).

3-7.1.1.2 **Address Latch**. At the start of a processor bus cycle, the processor outputs a logic "1" ALE (Address Latch Enable) signal which allows address latch U7 to accept the lower order address (AO-A7) appearing on the time-multiplexed data/address bus (AD0-AD7). After the lower order address byte has been latched, ALE goes low (logic "0"). This switches the latch into the "hold" condition in which it holds the lower order address byte on the A0-A7 output bus until the next bus cycle.

3-7.1.1.3 **Watchdog Timer and Lockout Circuit**. The watchdog timer and lockout circuit automatically resets the processor, multi-protocol serial controller, and display circuits if there is a software problem or if input power is too low.

3-7 1.1.3 1 **Watchdog Timer** A 19.2 kHz clock from the modem circuit is fed to the CK* (Clock) input of a 14-bit counter (U18). Operational software contains output instructions inserted at intervals into the code which performs access to address location 40 of the I/O memory space, causing the WDTR* chip select signal to pulse low. This pulse, via R25 and Q2, resets U18 to zero before it reaches a count of 8,192, when its Q14 output goes high. If, for any reason, software is not executing properly, the WDTR* signal will not be generated and the counter will be allowed to count up until its Q14 output goes high (logic "1") 426 milliseconds after its last WDTR* pulse.

The logic "1" 1 Hz pulse now appearing at the Q14 output of U18 is fed through the Watchdog Enable Jumper (E4) to pin 6 of NOR gate U14, resulting in a logic "0" RESET* pulse at U14, pin 4 which is fed to the I/O function and the display circuits. The RESET* signal is also inverted by U14-1 to provide a logic "1" RESET pulse to the processor and to the display circuits. The WDTR* signal can be monitored at TP18 on the microprocessor PCBA. When standard operational software is executing properly, the watchdog will never 'time-out' and reset the processor, because the software resets the counter at intervals less than 426 milliseconds. Any fault condition which causes normal execution of some software to be disrupted, including many hardware faults, transient electrical abnormalities and some software bugs, will cause a watchdog time-out and subsequent reset.

3-7.1.1.3.2 **Lockout Circuit**. The lockout circuit generates signals which initialize the processor and lock out the processor from the RAM and real-time clock whenever input power is low. When a power failure, brown-out, or power-down occurs, the lockout circuit detects the condition before the +5V supply voltage to the digital logic drops below 4.75V and de-selects both the real-time clock and RAM, preventing their contents from being changed. Simultaneously, the microprocessor chip is reset. When power returns to normal operating levels, the processor is released from reset and starts executing software at its reset initialization address. The RAM and real-time clock are re-enabled for CPU address. Resistors R27, and R28 form a voltage divider which keeps transistor Q3 turned on when the unregulated input voltage (VUNR) is above approximately +7.75v. With Q3 on, the logic "0" level at its collector keeps inverter gate U6-10 off. The resulting high (logic "1") CLO signal at U6, pin 10 produces a logic "0" UNV signal at U6, pin 8. This logic "0" signal causes the LKOUT* signal at U11, pin 6 to go high. It also causes the SLO* signal at U11, pin 11 to go high, thereby causing the LKOUT signal at U1, pin 8 to go low. Thus, during normal operation, LKOUT* will be high and LKOUT will be low. The LKOUT* signal can be monitored at TP15 on the microprocessor PCBA. Zener diode CR10 sets the threshold level at which Q3 turns off. If the AC power input to the indicator/recorder is interrupted, VUNR drops. When it drops to the threshold level set by CR10, Q3 turns off to the point where its collector voltage swings sufficiently positive to turn on inverter gate U6-10 and CLO is now at the logic "0" level.

The ALE (Address Latch Enable) signal generated at the start of a processor cycle enables NAND gate U11-11. With U11-11 enabled, the logic "1" UNV signal at U6, pin 8 will cause the resulting low SLO* output of U11-11 to set the lockout latch. The logic "1" LKOUT signal now appearing at U11, pin 8 is fed to pin 5 of NOR gate U14 in the watchdog timer and the RESET and RESET* signals are generated by U14-4 and U14-1 as described in paragraphs 3-7.1 1.3.1 The LKOUT* signal generated at U11, pin 6 locks the processor from the RAM and real-time clock during a power interruption. The ALE signal must be high to set LKOUT, ensuring that the lockout does not occur during the middle of a processor bus access. If the processor is writing to memory, it gives it a chance to finish writing. Otherwise, data which should have been written might be disrupted.

The GND pin of U11 is tied to VBAT, which is approximately 0.2V above ground when AC power is on. When AC power is off, VBAT goes to -2.7V below ground, so LKOUT* goes to near -2 7V as well to provide battery backup power to, and de-select the real-time clock and the RAM.

3-7.1.1.4 **Clock Generator**. The clock generator uses a 14.7456 MHz crystal (Y3) to generate a 14.7456 MHz squarewave. The 14.7456 MHz squarewave is divided by three in a 4-bit binary counter (U16) to provide a 4.9152 MHz clock, whose frequency is just slightly under the 5 MHz maximum of the 80C88 processor. This clock is asymmetrical, high for one-third of the time and low for two-thirds of the time. The 14.7456 MHz squarewave is also divided by six in U16 to provide a 2.4576 MHz peripheral clock which is provided to the I/O function, inter-assembly communications function, and the display circuits.

3-7.1.1.5 **Memory Chip Select Decoder**. The 80C88 processor generates 20-bit memory addresses, addressing up to 1 Megabyte of memory. The microprocessor PCBA needs at most 32K bytes of EPROM and 32K bytes of RAM, so it ignores the high four address bits (A16-A20) and decodes only A0-A15 to implement a 64K byte memory address space The memory chip select decoder uses three NOR gates (U17-10, U17-13, U17-4) to generate chip select signals for the RAM (RAMCS*) and EPROM (EPCS*) These chip select signals divide memory selection into two 32K byte segments, RAM being the lower order 32K bytes from 0000 to 7FFF hexadecimal and EPROM being the high order 32K bytes from 8000 to FFFF hexadecimal.

When accessing lower order 32K of memory, the processor outputs a logic "0" on A15 and a logic "0" on IO/M*, causing U17, pin 10 to go high (logic "1") and U17, pin 13 (RAMCS*) to go high (logic "1"). RAMCS* applied to the CS* (chip select) input of the RAM enables the RAM for the lower 32K of memory. When address bit A15 goes high (logic "1"), a logic "0" EPCE* chip select is generated at U17, pin 4. This signal, applied to the CE* (chip enable) input of the EPROM, enables it for the high 32K of memory. The EPCS* signal can be monitored at TP17. Since IO/M* is not decoded in generating EPCE*, the EPROM can also be accessed in IO space, although this capability is not used.

3.7.1.1.6 **RAM**. The microprocessor PCBA uses a type 6264 8K x 8 RAM (Random Access Memory) chip (U8) as the scratchpad memory for the 80C88 processor. The microprocessor PCBA can also be set up to use a 32k x 8 type 62256 RAM; however, there is no defined use for the larger RAM at this time, since all specified functions can be performed within the 8K x 8 chip. To accommodate the larger RAM, the printed circuit trace between pins 2 and 3 (LKOUT*) of E3 must be cut, and a jumper wire installed between pins 1 (A14) and 2 of E3.

Note that the RAM contents may be lost during power-down using the larger RAM since the LKOUT* disable is replaced with A14. RAM chip U8 is enabled by the RAMCS* chip select signal from the memory chip select decoder (paragraph 3-7.1 1.5) during accesses to the low 32K bytes of memory. Address lines A0-A14 are used to select the location in the RAM that is to be accessed. Data are written into or read from memory depending on the WR* (Write) or RD* (Read) signals from the processor. These signals are logic "0" when active. During a power interruption, the CS1*, RD*, and WR* inputs to the RAM may go to unpredictable levels, potentially causing the data in the RAM to change erroneously. To prevent this from happening, the lockout circuit pulls LKOUT* low, thereby pulling the RAM's CSA input low and inhibiting any further accesses to the RAM until power returns to proper levels. During a power interruption, data in the RAM are not lost since the RAM will be powered by the battery backup circuit via the VBAT lead which is connected to the RAM's GND terminal. Data transfer between the RAM and processor is via the multiplexed data/address bus (AD0-AD7).

3-7.1.1.7. **EPROM**. All software for the indicator is stored in an erasable and programmable read-only memory (EPROM). The EPROM is mounted in a socket so that it can be replaced in the field when a software change is needed. The microprocessor PCBA can be configured with either a type 27128A 16K x 8 or type 27256 32K x 8 EPROM chip (U9). All specified functions are performed using the 16K x 8 EPROM, and there is no defined use for the larger EPROM at this time. To use the larger EPROM, the printed circuit trace from pin 1 to pin 2 of E2 must be cut and pins 2 and 3 of E2 must be jumpered. The EPROM (Erasable Programmable Read Only Memory) is the program storage for the 80C88 processor.

There are two control signals provided to the EPROM, EPCS* (EPROM Chip Select) and RD* (Read). Both signals have to be low (logic "0") before program information in the EPROM can be read back to the processor via the multiplexed data/address bus (AD0-AD7). The EPROM is enabled by EPCS* during accesses to the lower order 32K of memory. Address lines A0-A14 are used to select the location in the EPROM that is to be accessed.

3-7.1.1.8 **I/O Chip Select**. A 1-of-8 decoder/demodulator (U15) is used to generate chip select signals for each peripheral when the processor is addressing each of the individual peripherals on the I/O cycle.

U15 has three enable inputs, two active low and one active high. Every output will be high unless the CS2* and CS3* pins are low and the CS1 pin is high. Setting the IO/M* signal at CSI high, the ALE signal at CS2* low, and the A15 address bit at CS3* low will enable U15. When enabled, U15 will decode address bits A5, A6, and A7 to drive one of the eight active low outputs (Y0-Y7) to a low (logic"0") level. The chip select signals generated are as follows:

U15 PIN	CHIP SELECT SIGNAL	IO PORT (hexadecimal)
Y0	MPSC* (Multi-Protocol Serial Controller)	0000-0001
Y1	RTC* (Real Time Clock)	0020-0031
Y2	WDTR* (Watchdog Timer Reset)	0040
Y5	KDC* (Keyboard/Display Controller)	00A0-00A1
Y6	PDQ* (Printer Data Qualifier)	00C0
Y7	MCS* (Miscellaneous Control and Status)	00E0

3-7.1.1.9 **Real-Time Clock**. The real-time clock circuit uses a 32.768 kHz crystal (Y2) to generate a 32.768 kHz clock. The 32.768 kHz clock is used to control counters within a real-time clock chip (U10) which keeps track of real time from 1/100 second to 99 years. An extremely stable oscillator frequency is achieved through the use of an on-chip regulated power supply.

The clock is set or read by accessing the eight internal separately addressable and programmable counters via the multiplexed data/address bus (AD0-AD7). Time is software selectable using the 24 hour format when the WR* (Write) signal from the processor is low. A low RD* (Read) signal is required to read real-time over the AD0-AD7 bus. Internal latches prevent clock rollover during a read cycle. Counter data is latched on the chip by reading the 1/100th seconds counter and is held indefinitely until the counter is read again, assuring a stable and reliable time.

The real-time clock generates an interrupt (RTCI*) every 100 milliseconds and at other intervals programmed by software. This interrupt maintains important timing relationships in software. The battery backup circuit powers the real-time clock in the event of a power failure or interruption. When a power-down or power failures occurs, the lockout circuit pulls LKOUT* low.

This keeps the real-time clock input/output and read/write functions disabled and limits its operation to time-keeping and interrupt generation, resulting in low power consumption and avoiding erroneous changes to the time counters. To achieve low power consumption during power-down, the VDD and VSS leads and the normal power and ground leads of U10 must be at ground and the VBKUP lead must be at -2 volts or lower. The watchdog circuit pulls LKOUT*, tied to VBKUP, to -2.7V from the backup battery when AC power is lost.

3-7.1.1.10 **Battery Backup Circuit**. (See FIGURE 19 of T.O. 31M1-2FMQ13-3.) During a power interruption, a 2.7V lithium iodide battery powers the RAM and real-time clock until AC power is restored. Unlike other types of lithium batteries, lithium iodide cells have a long life and are not subject to explosion; however, they are not rechargeable and are soldered into the microprocessor PCBA. Therefore, care must be taken to avoid unintentional discharge. Jumper E1 should be disconnected when the microprocessor PCBA will not be getting AC power for more than a few days. The battery's 0.65 ampere-hour capacity will typically last 13,000 hours (18 months) under the load of 50 microamperes drawn by the RAM and the clock when AC power is off.

3-7.1.2 **I/O Function**. (See FIGURE 20 of T.O. 31M1-2FMQ13-3.). As shown in FIGURE 20 of T.O. 31M1-2FMQ13-3, the I/O function is comprised of a multi-protocol serial controller (U4), line drivers (U13), and line receivers (U3). The multi-protocol serial controller (MPSC) includes a universal synchronous/asynchronous receiver transmitter (USART). The line drivers and receiver are compatible with MIL-STD-188-114.

a. Converts parallel data from the multiplexed data/address bus (AD0-AD7) into serial asynchronous serial bit streams for transmission by the modem in the inter-assembly communications function and converts serial bit streams from the modem into parallel form for processing by the processor.

b. Converts parallel data from the multiplexed data/address bus (AD0-AD7) into serial asynchronous serial bit streams for transmission to the AWDS port, and converts asynchronous serial bit streams from the AWDS port into parallel form for processing by the processor.

c. Adds the necessary start and stop bits to each character to be transmitted, and strips off these characters from the received characters.

d. Generates processor interrupt and provides interrupt vectors when serial data bytes are sent and received and when external signals change state.

The MPSC comprises system control logic, interrupt controller function, and two independent communication channels, side-A and side-B. These circuits are described in the following paragraphs.

3-7.1.2.1.1 **System Control Logic**. The system control logic function of the MPSC controls all operations performed by the MPSC in response to the signals from the processor. Operation of the MPSC is controlled by the clock generator in the CPU function. The 2.4576 MHz clock to the CLK pin is the system clock and is used for timing of the MPSC's internal functions. This clock must be slower than the 4.9152 MHz processor but considerably faster than the 1200 bps bit rate.

Transfer of information between the processor and MPSC is controlled by RD* (Read) and WR* (Write) strobes provided by the processor. A RD* strobe controls a data byte or status byte transfer from the MPSC to the CPU. A WR* strobe controls transfer of data or commands to the processor.

A logic "0" MPSC* chip select signal from the processor selects the MPSC and enables reading from and writing into the registers.

3-7.1.2.1.2 **Interrupt Controller Function**. The MPSC includes a built-in interrupt controller function which generates six different vectored interrupts on different USART internal or external conditions. The following paragraphs describe the source, purpose, type, priority, and required response for each interrupt.

a. **Inter-Assembly Receiver Interrupt**. This interrupt is generated when a character is received via the inter-assembly communications function (side-A). This is an interrupt for the purpose of processing received characters and has the highest priority level. The interrupt rate will be once every 8.33 milliseconds during receipt of messages.

b. **Inter-Assembly Transmit Interrupt**. An interrupt occurs each time a character is transmitted when the MPSC side-A transmit buffer becomes empty. The interrupt is second in priority and will occur at a rate of 8.33 milliseconds during data transmission periods. This would occur only in master or backup indicators/recorders.

c. **AWDS Receiver Interrupt**. This interrupt is generated when a character is received at the beginning of each AWDS output message due to the built-in test loopback circuits. The side-B channel is used for the AWDS port. It is third in priority. The highest interrupt rate would be approximately once every 100 milliseconds for a four-sensor system.

d. **AWDS Transmitter Interrupts**. An interrupt occurs each time a character is transmitted when the MPSC side-B buffer becomes empty. This occurs approximately 110 times during each AWDS message for each sensor. The interrupt rate is once every 8.33 milliseconds during transmission periods. This interrupt is fourth in priority.

e. **Inter-Assembly External Status Interrupt**. This interrupt can be generated in three events: 1) change of the state of Carrier Detect, 2) a Real-Time Clock Interrupt, or 3) Front Panel Switch Interrupt. A change in Carrier Detect status is used to detect the beginning and the end of the receipt of a message. The Real-Time Clock is used to sequence scheduled events and requires determination of the time interval that caused the interrupt. The real-time clock interrupts once each 100 milliseconds and is the prevalent interrupt of the three. A front panel interrupt is generated whenever a front panel pushbutton is pressed. This interrupt is fifth in priority.

f. **AWDS External/Status Interrupt**. This interrupt is generated when there is a change in DM, CS, or TM control lines of the AWDS RS-449 interface. The status of the three lines controls the AWDS output routine. This interrupt has the lowest priority. The service routine records the state of the interface line for use by the AWDS output. The frequency of this interrupt is very low.

3-7.1.2.1.3 **Channel A Communications**. Channel A of the MPSC (U4) interfaces the 8-bit multiplexed data/address bus with the modem in the inter-assembly communications function. A low (logic "0") CD* (Carrier Detect) signal from the modem indicates that a data carrier signal has been detected and that a valid signal is present on its RXDa line.

Receipt of a low CD* signal on channel A causes the INT* (Interrupt) pin of the MPSC to go low. This is inverted to logic "1" by U6-6 and applied to the INTR pin of the processor. The processor selects the MPSC by causing a logic "0" MPSC* chip select to be placed on the CS* pin and a logic "0" RD* strobe on the RD* pin. A low RD* strobe informs the MPSC that the processor is inputting data or status information. Channel A of the MPSC is selected when the A0 address bit is low.

The receive function begins when a low RTS* (Request-To-Send) signal is fed to the RTS* pin of the MPSC by the modem. A valid start bit is detected if a low persists for at least 1/2 bit time on the Receive Data (RXDa) input. The data is sampled at mid-bit time, on the rising edge of the Receive Clock (RXCa), until the entire character is assembled.

Data from the modem comes in serially to the MPSC RXDa pin. The MPSC strips off the start and stop bits and provides data from the modem to the processor in parallel form via the AD0-AD7 bus. An interrupt can also be generated, thereby initiating transmission of data, whenever the CTS* pin or SYNCDETa* pin is driven low. The CTSa* pin receives a low RTCI* (Real-Time Clock Interrupt) signal from the real-time clock every 100 milliseconds and at other times dictated by the software. The SYNCDETa* pin receives a low KDCI* (Keyboard Display Controller Interrupt) whenever a front panel pushbutton is pressed. Upon being instructed that the MPSC is ready to receive data from the processor, the processor selects the MPSC by causing a logic "0" MPSC* chip select to be placed on the CS* pin and a low WR* strobe on the WR* pin. A low WR* strobe informs the MPSC that the processor is outputting data or commands to the MPSC. The MPSC then converts the parallel data from the processor into a continuous serial data stream. Transmit data is fed serially to the modem via the TXDa pin. Serial data are fed from the TXDa pin on the trailing edge of the Transmit Clock (TXC). The MPSC adds a start bit and stop bit to every byte that is transmitted. Thus, the complete transmitted character includes a start bit, eight data bits, and a stop bit. Both RXC and TXC clocks are 19.2 kHz clocks, which is 16 times the 1200 bps bit rate used for transmitting and receiving data. This 19,200 Hz clock is used to detect the beginning of a start bit and end of a stop bit. Then it counts 16 clock pulses to find each bit thereafter. Since the MPSC is programmed to operate asynchronously, it does not require a clock to be transmitted with the data. By using the 16x clock, the MPSC can determine the state of each bit.

3-7.1.2.1.4 **Channel B Communications**. Channel B of the MPSC (U4) interfaces the 8-bit multiplexed data/address bus with the AWDS port. A low (logic"0") CD* (Carrier Detect) signal from the AWDS port indicates a Data Carrier signal has been detected. Receipt of a low CDb* signal on channel B causes the INT* (Interrupt) pin of the MPSC to go low. The processor selects the MPSC by causing a logic "0" MPSC chip select to be placed on the CS* pin and a low RD* strobe on the RD* pin. A low RD* strobe informs the MPSC that the processor is inputting data or status information. Channel B of the MPSC is selected when the A0 address bit is high. A valid start bit is detected if a low persists for at least 1/2 bit time on the Receive Data (RXDb) input. The data is sampled at mid-bit time, on the rising edge of the Receive Clock (RXC), until the entire character is assembled.

Data from the AWDS port comes in serially to the MPSC RXDb (Receive Data) pin. The MPSC strips off the start and stop bits and provides data from the AWDS port to the processor in parallel. When SYNCDETb* and CTSb* are both low, the MPSC goes to its ready state. This enables the MPSC to convert parallel data from the processor into serial form for transmission to the AWDS port. Upon being instructed that the MPSC is ready to receive data from the processor, the processor selects the MPSC by causing a logic "0" MPSC chip select signal to be placed on the CS* pin and a logic "0" WR* strobe on the WR* pin. A low WR* strobe informs the MPSC that the processor is outputting data or commands to the MPSC. The MPSC then converts the parallel data from the processor into a continuous data stream. Transmit data is fed serially to the AWDS port via the TXDb pin. Serial data are fed from the TXDb pin on the trailing edge of the Transmit Clock (TXC). The MPSC adds a start bit and stop bit to every byte that is transmitted Thus, the complete transmitted character includes a start bit, eight data bits, and a stop bit.

When CTSb* goes false (logic "1"), this will automatically stop transmitting from the TXDb pin. Thus, the processor doesn't have to come in and tell it to stop transmitting. This will be done automatically within the MPSC when the CTSb* input to the MPSC, provided via inverters U17-1 and U6-12, goes high. The MPSC provides a low DTR* (Data Terminal Ready) signal to the AWDS port when outputting transmit data.

3-7.1.2.2 **AWDS Port**. The AWDS port consists of an RS-449 AWDS connector (A3J4), RS-422 line receivers, and RS-423 line drivers RS 449 specifies a 37 pin D connector and covers the mechanical specifications and circuit descriptions, and uses the electrical characteristics specified in RS-442 (balanced Circuits) and RS-423 (unbalanced circuits). RS-449 devices can be interconnected with RS-232-C devices using the proper cabling. AWDS connector A3J4 accommodates four balanced receive inputs. Each receive input is applied to an RS-422 line receiver in a quad differential line receiver (U3) which converts RS-422 logic levels to +5V TTL logic levels used by the MPSC. U3 can be made to receive single-ended inputs by connecting the appropriate differential lead to ground. That can be done in the external cabling to AWDS connector A3J4 by providing a ground to the second lead of the differential pair. This provides flexibility in interfacing the wind measuring set to RS-449 equipment that use either single-ended or differential mode transmission. The 10K resistors on the inputs of U3 set the level of the input signals to a known state when nothing is connected to the AWDS port. Transmit data (ATXDa) and Data Terminal Ready (ARS*) signals from the MPSC are fed to AWDS connector A3J4 via a single-ended RS-423 line driver (U13). This line driver converts the +5V TTL logic level of the signal from the MPSC to RS-423 levels. A 10K resistor (R33) provides loopback of the TXD signal to the RXD input for built-in test. This allows the software to transmit a byte and check whether it was transmitted correctly. Since the AWDS port is specified as an RS-449 send only mode interface, it has no requirement to receive data on the RDA and RDB inputs. During normal operation, the RDA and RDB inputs to the AWDS port should be left open to allow the bit to function normally; otherwise, the status code display indicates an AWDS port fault when the circuit is working correctly.

The indicator and recorder hardware has the capability to receive data through the AWDS port on the RDA and RDB inputs. This capability, although not usable with operational software in EPROM, may be used with special test software in a special EPROM during a manufacturing test or depot repair.

3-7.1.3 Inter-Assembly Communications Function. (See FIGURE 21 of T.O. 31M1-2FMQ13-3.) As shown in FIGURE 21 to T.O. 31M1-2FMQ13-3, the inter-assembly communications function is comprised of a Bell 202-type modem and a line termination circuit. Each of these functions is described in the following paragraphs.

3-7.1.3.1 **Modem**. The inter-assembly communications function uses a single chip asynchronous FSK (Frequency Shift Keying) voiceband modem (U1) which operates at 1200 bps. It uses silicon gate CMOS technology to implement a switched capacitor architecture. The modem's transmitter is a programmable frequency synthesizer that provides one of two output frequencies on TXA representing the marks (1200 Hz) and spaces (2200 Hz) (which correspond to a logic "1" or a logic "0", respectively) on the TXD input. The receive section of the modem demodulates analog signal appearing at the RXA input and is based on the principle of frequency-to-voltage conversion. This section contains a group delay equalizer (to correct phase distortion), automatic gain control, carrier detect level adjustment, thereby optimizing performance and giving a low bit error rate.

The carrier detect circuit sets CDT output high if the level of received in-band energy is above a value set on the CDL input by Carrier Detect Threshold adjust potentiometer R2. Potentiometer R1 is the Receive Bias Distortion adjustment control, and is used to set the duty cyucle on RXD to 50% when a 50% duty cycle TXD signal is transmitted and looped back.

The modem uses an external 4.4336 MHz crystal (Y1) frequency source. This crystal frequency drives an internal programmable frequency synthesizer that drives the output frequencies by variables of the 4.336 MHz oscillator frequency. An on-chip oscillator runs from the external 4.4336 MHz crystal connected between the OSC1 and OSC2 pins to provide a 19.2 kHz clock from the CLK output, which is 16 times the highest selected bit rate (transmit or receive). This 19.2 kHz clock is fed via inverter U6-4 to the TRS pin which sets the standard bit rates and mark/space frequencies.

3-7 1.3.2 **Line Termination Circuit**. The line termination circuit uses four operational amplifiers (U12-14, U12-1) in a single chip to provide gain adjustment, power drive capability, and anti-streaming control. The modem and line termination circuit are operated from a +5V analog supply (A+5).

The TXA output of the modem is coupled through capacitor C5 and resistor R8 to operational amplifier U12-1. Potentiometer R3 is the Transmit Level adjust potentiometer. Potentiometer R3, in conjunction with resistor R8, sets the gain of operational amplifier U12-1 to the 0 dBm output level (2.2V peak-to-peak). Q1 is a JFET (Junction Field Effect Transistor) which is controlled by the output of U12-8.

Operational amplifiers U12-7 and U12-8 provide anti-streaming timeout and level shifting functions in the control of Q1, under processor control, via the RTS* output of USART U4. When RTS* is set low by software, the gate of Q1 is pulled to +5V thorough 10K resistor R13, thus turning Q1 on and connecting U12-1 output to T1 for transmission on the inter-assembly wiring. If RTS* stays low for more than about a second, the RC time constant of R11 and C7 is exceeded and the gate of Q1 is pulled to -12V, turning Q1 off and releasing the inter-assembly channel so that another assembly can transmit. The RC timeout protects the entire system from being disabled by a fault in a single assembly that keeps RTS* low and would otherwise allow the single faulty assembly to continuously "stream" its modem output onto the inter-assembly wiring, thus disrupting any other assembly's transmission. When software completes a transmission, it normally sets RTS* back high, which immediately turns Q1 off and quickly discharges C7 through CR1 so that C7 is again ready to time the next RTS* pulse.

The Carrier On jumper (E5) must be disconnected when installed in an operational wind measuring set, but may be connected during depot repair or field installation to continuously enable the modem's output onto the inter-assembly wiring for test purposes. During depot repair, E5 can be connected to provide a test signal for test, calibration, and troubleshooting.

During installation, E5 can be connected to provide a constant test signal to check out the inter-assembly wiring for opens, shorts, reflections, high loads, etc. Transformer T1 couples data transmitted by U12-1 onto the inter-assembly wiring, D1(T) and D2(R), through connector J3. Zener diode CR3, connected across the transformer, provides transient suppression. It will take lightning pulses from the inter-assembly and short them out before they can damage the line termination circuits.

Data from the inter-assembly wiring, D1(T) and D2(R), comes in through J3 to transformer T1, which AC couples the receive data to operational amplifier U12-14. The receive level is set by potentiometer R4 in combination with resistor R12. The output of U12-14 is coupled through capacitor C6 into the RXA pin of the modem for demodulation.

3-7.2 **Display PCBA**. The following paragraphs provide a detailed description of each of the major functions comprising the display PCBA used in the indicator and recorder. There are minor differences between the display PCBA used in the indicator and the display PCBA used in the recorder. Unless otherwise indicated, the following descriptions apply to both configurations.

3-7.2.1 **Display Controller and Keyboard Scanner**. (See FIGURE 22, Sheet 3, of T.O. 31M1-2FMQ13-3.) The display PCBA uses a type 8279-5 programmable keyboard and display interface (U3). The keyboard portion provides a scanned interface to all front panel pushbuttons used by the operator, as well as to most configuration jumpers. A pushbutton depression sets the KDCI (Keyboard/Display Controller Interrupt) interrupt line to the MPSC in the I/O function. The display portion provides a scanned display interface for the 7-segment LEDs. U3 includes a 16 x 8 display RAM which is organized as a dual 16 x 4 RAM. This RAM can be loaded or interrogated by the processor via the multiplexed data/address bus (AD0-AD7.) Both read and write of the display RAM may be done with auto-increment of the RAM address. A description of the 8279-5 pin function is given below:

PIN	DESCRIPTION
DB0-DB7	Bi-Directional Data Bus. All data and commands between the processor and the 8279-5 are transmitted on these lines.
CLK	Receives the 2.4576 MHz clock. This clock is used to generate internal timing.
RESET	A high RESET signal on this pin resets the 8279-5.
CS	Chip Select. A low on this pin enables the interface functions to receive or transmit.
A0	Buffer Address. A high on this line indicates the signals in or out are interrupted as a command or status. A low indicates that they are data.
RD*, WR*	Input/Output Read and Write. These signals enable the data buffer to either send data to the external bus or receive it from the external bus.
IRQ	Interrupt Request. Provides a high KDCI (Keyboard Display Controller Interrupt) to the MPSC when a front panel pushbutton is pressed.
SLO-SL3	Scan Line outputs which are used to scan the switch matrix and the display digits. These lines are binary encoded to select each of 16 different display digit pairs.
RLO-RL7	Return Line inputs which are connected to the scan lines through switches. They have active internal pullups to keep them high until a switch closure pulls one low.
SHIFT	The Shift Input Status is stored along with the key position on key closure in the scanned keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.
CNTL	For keyboard modes, this input is used as a control input and stored like status on a key closure.

PIN	DESCRIPTION
OUT A0-OUT A3, OUT B0-OUT B3	Two multiplexed output ports. Data from these outputs are synchronized to the scan lines (SL0-SL3). Continually cycle through two pairs of 4-bit words which, at any one time, will activate one LED in bank A and one LED in bank B.
BD*	This Bank Display output is used to blank the display during digit switching or by a display blanking command.

3-7.2.2 **BCD-to-7-Segment Decoders**. Two BCD-to-7-Segment decoders (U14,U15) are used to decode the two multiplexed BCD inputs from the display controller and keyboard scanner to two sets of 7-segment outputs. The outputs of U14 and U15 determine which segments in the 7-segment displays are turned on for each BCD input. The LAMP TEST pushbutton (S9) will turn on all segments of each 7-segment display when pressed, causing the number 8 to be displayed on each display.

3-7.2.3 **Current Sources**. (See FIGURE 22, Sheet 3, of T.O. 31M1-2FMQ13-3.) A current source, consisting of an operational amplifier and a PNP transistor, is provided for each of the 14 segment outputs. The 14 current sources are comprised of quad operational amplifiers U10-U13 and transistors Q1-Q14. The output of the current source is proportional to the input VI REF. Current is controlled by regulating the voltage across the 3.3 ohm resistor. When turned on by the corresponding output of the BCD-to-7-segment decoder, each current source will provide approximately 200 milliamperes current drive to display the segments.

3-7.2.4 **7-Segment LED Displays**. (See FIGURE 22, Sheet 3, of T.O. 31M1-2FMQ13-3.) The display PCBA uses 32 type-HDSP5533 7-segment displays, which are arranged in two banks of 16 each. All the anodes of the LEDs in bank A are driven simultaneously and all the anodes of the LEDs in bank B are driven simultaneously by the current sources. The cathodes of the LEDs are grounded through a transistor switch in the digit select circuit to allow current to flow through it. Only one cathode in each LED bank can be grounded at a time. Thus, only one LED in each bank carries current pulses at a time.

While the display controller and keyboard scanner is multiplexing, it will drive one LED in Bank A and one LED in bank B simultaneously. Then it continues with the next pair in sequence to the end, then it starts over again. This occurs at a rate of 267 times per second. The human eye averages the resulting light pulses, so it appears that the LED's brightness is constant.

3-7.2.5 **Digit Select**. (See FIGURE 22, Sheet 3, of T.O 31M1-2FMQ13-3.) The digit select circuit uses two 1-of-8 decoders (U7, U8) to provide a 1-of-16 output corresponding to the BCD scan address outputs (SL0-SL3) from the 8279-5 (U3). The two 1-of-8 decoders are combined by using the SL3 output as the data input to the decoders as follows. SL3 is the most significant bit of the scan line output. SL3 is connected directly to the data input (D) of U7. The data input (D) of decoder (U8) is connected to SL3 after being inverted by U2. This arrangement causes the output of U8 to be a logic "0" when SL3 is a logic "1." The output of U7 is a logic "0" when SL3 is a logic "0." As the count sequence of SLO-SL3 proceeds from 0 to 15, SL3 is a logic "0" which makes the data input (D) to U8 a logic "1." Each output of U8 will match the data input (D) when selected by the scan lines SL0-SL2. When the count reaches the value "8" SL3 becomes a logic "1" and the data input (D) to U7 becomes a logic "1" while the data input to U8 becomes a logic "0." As the count proceeds each output of U7 will match the data input (D) when selected by the scan lines SLO-SL2. The combined actions of U7 and U8 provide a 1-of-16 decoder function. A logic "1" output from the 1-of-16 decoder turns one of the transistor switches (Q17-Q29) which grounds the cathode of one LED in bank A and one LED in bank B to turn on that 7-segment LED display. These transistors will sink approximately 3 amperes of current.

3-7.2.6 **Intensity Control**. (See FIGURE 22, Sheet 3, of T.O. 31M1-2FMQ13-3.). The intensity of the 7-segment displays is controlled by changing the amount of current provided by the current sources to the LED segments. The set point of the current source is established by the voltage level at the signal labeled V1 REF. V1 REF is geenerated by one of the operational amplifiers of U10 configured as a voltage follower. The voltage follower is connected to the intensity potentiometer located on the front panel. Output of the current sources increases as V1 REF increases. Q31 turns off the current sources when a reset occurs

3-7.2.7 **Printer Port Latches**. (See FIGURE 22, Sheet 1, of T.O. 31M1-2FMQ13-3.). The printer port is located on the display PCBA but is not related to the display function. It is only used on the dash 2 indicator configuration.

The printer port uses two latches (U4 and U5) and a bus driver (U6) to interface the AD0-AD7 bus with the printer connected to PRINTER connector A3J3. Latches U4 and U5 are output latches and are controlled by the WR* strobe from the processor. Bus driver U6 drives inputs from the printer on AD0-AD7, and is controlled by the RD* strobe from the processor.

Latch U5 provides the eight data bits (PD0-PD7) to the printer. Latch U4 provides two additional outputs (STRB*, PRM*) for the printer. STRB* is used to strobe the data into the printer. This occurs after the data lines of the printer port latches have been set. PRM* is used to initialize (prime) the printer during power-up operations. Latch U4 also provides an ALRM* output to the alarm circuit and provides four outputs which control the SENSOR SELECT LEDs. Bus driver U6 receives inputs from the printer including ACK* (Acknowledge), BUSY, PAPMT (Paper Empty) SLCT (Select), and FAULT* Latch U6 has a strap option which can be strapped on E1 to let the processor software know whether to compute wind direction and speed averages on a 2- minute or 10-minute basis.

3-7.2.8 **Alarm**. (See FIGURE 22, Sheet 1, of T.O. 31M1-2FMQ13-3.) The dash 2 indicator configuration includes an alarm circuit which sounds a piezo-electric audible alarm when enabled by the processor. When the processor software detects that the active sensor has been changed, it causes the ALRM* output of printer port latch U4 to go low. When ALRM* is low, U1 is enabled and will produce a 3.85 kHz square wave across piezo-electric alarm TX1, causing a loud audible tone of 3.85 kHz with overtones.

Diodes CR1-CR4 protect the alarm. The piezo-electric element is normally an output transducer, but can function as an input transducer as well. If the display PCBA received a mechanical shock, voltage pulses would be induced which could damage U1. To prevent this, diodes CR1-CR4 clamp the voltage transients to +5V or ground.

3-7.2.9 **Keyboard Scanner**. FIGURE 22, Sheet 3, of T.O. 31M1-2FMQ13-3 shows the operator pushbuttons which are mounted on the front panel. These pushbuttons are continually scanned by the output of a 1-of-8 decoder (U9). This chip decodes the SL0, SL1, and SL2 Scan Line inputs from the 8279-5 (U3). When a pushbutton has been pressed, an output is sent back to the 8279-5 (U3) via the RL0-RL7 Return Lines.

3-7.3 **Power Supply and Distribution**. (See FIGURE 23 of T.O. 31M1-2FMQ13-3.) FIGURE 21 of T.O. 31M1-2FMQ13-3 shows the indicator/indicator power supply and distribution circuits. The indicator/recorder power supplies operate from either 115 VAC or 230 VAC, 47-60 Hz, single phase.

The AC input voltage is fed into the indicator/recorder via an EMI filter (FL1) and POWER circuit breaker CB1. During installation, optional jumpers (E32) are connected for either 115 VAC or 230 VAC operation.

The AC input is then fed to a transient suppressor circuit (on the interconnect PCBA) comprising two varistors (RV3, RV4), two gas tubes (E30, E31), and two 5W wirewound resistors (R5, R6). The varistors have a fast response time but low power dissipation. On the other hand, the gas tubes have a high power dissipation but slow response time. By using a combination of varistors and gas tubes, the transient suppressor circuit provides fast response to transients, while providing the required power dissipation.

When a transient appears on the AC input, varistors RV3 and RV4 turn on quickly to clamp the transients on the AC input to an acceptable level. Gas tubes E30 and E31 then turn on to dissipate most of the energy, and the varistors are relieved of this burden. Resistors R5 and R6 limit current through the gas tubes.

From the transient suppressor, the AC power is fed via J5 to two primaries in the transformer assembly. The transformer steps the AC input voltage down to a center-tapped 31 VAC and 10 VAC. The transformer assembly includes a full-wave rectifier (CR1) which provides rectification of the AC input voltage. The unregulated DC output voltage of this full-wave rectifier is fed via filter capacitors to the input of three linear voltage regulators. The two chassis mounted regulators provide VLED (+5.25 VDC at up to 3 amperes) and D+5V (+5.0 VDC at .1 ampere). Regulator U21 on the microprocessor PCBA provides A+5V (+5.0 VDC at .50 milliamperes).

The 31 VAC output of the step-down transformer is fed to a full-wave bridge rectifier on the microprocessor PCBA. The output of this full-wave rectifier is capacitor filtered and regulated by linear voltage regulators U19 and U20 to provide +12 VDC at 50 milliamperes and -12 VDC at 50 milliamperes.

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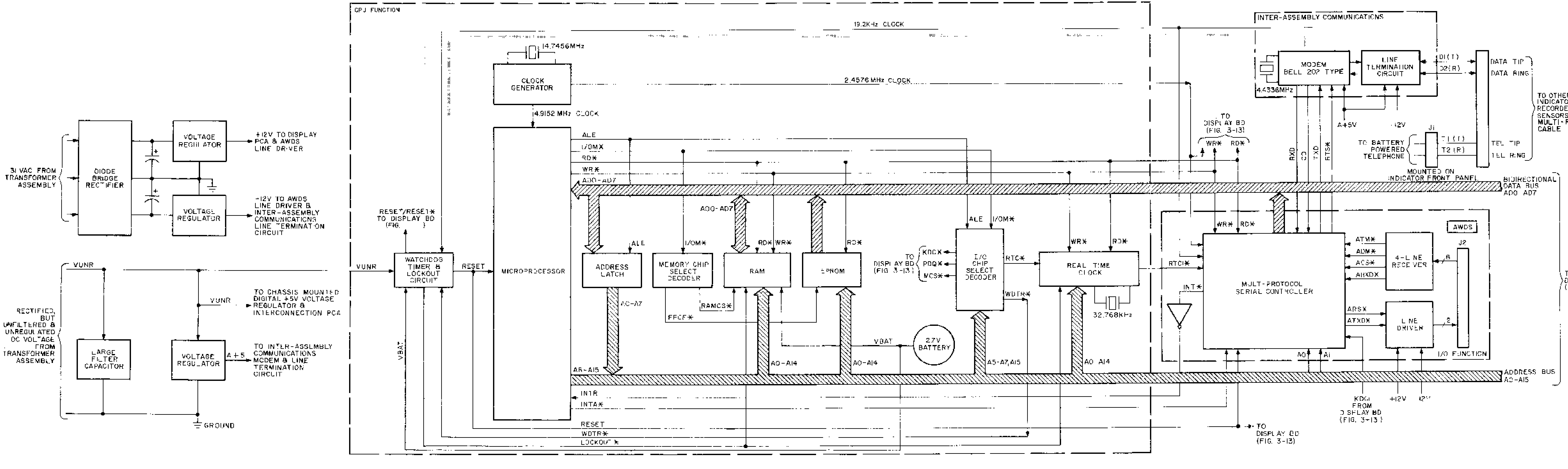

FO-1. Indicator/Recorder - Microprocessor PCBA, Block Diagram